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REVIEW

Plasma-based processes and thin film equipment for nano-scale device fabrication

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Abstract Plasma-based thin film equipment and processes have been widely used for micro-electronics, information storage sensors, and energy harvest/storage devices. To achieve higher package density, large storage capacity, and to meet other specific stringent design criteria, the film layer thickness is often reduced to a few nanometers or even to a few angstroms, while the device dimension has been shrinking to sub-micrometer scales. As the material thickness (h) approaches atomic dimension and the device dimension ($w \times d$) approaches a few tens of nanometers, thin film layer uniformity and inter-layer mixing, as well as device edge damage control are crucial for its performance and reliability. In this review paper, we will discuss briefly vacuum and plasma aspects, followed by a detailed review on various plasma-based thin film deposition and removal techniques. The deposition methods discussed here include magnetron sputtering, ion beam deposition (IBD), and plasma enhanced chemical vapor deposition (PECVD). We focus on the advantages and disadvantages of various hardware configurations and how to achieve uniform film growth over large area with minimized interlayer mixing for any specific process. The device patterning aspects cover ion beam etching (IBE), reactive ion etching (RIE), and various techniques for end-point detection of etching processes. We discuss how the definition technique affects edge damage, profile, and dimension ($w \times d$) control, as well as post-definition corrosion behavior. Some specific examples will be presented to highlight how the physical principles can be used in practice for film/device property control.

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Introduction

Film layer formation and removal steps are ultimately required in order to obtain functional devices or device arrays with designed dimensions. Figure 1 represents a typical process flow chart for nano-device fabrication, which highlights the important role of thin film deposition and removal steps. In this review, we will first briefly discuss the importance of background impurity control for ultra thin film processes and the major plasma sources available. We will then focus on various plasma-based thin film deposition equipment and processes used for active function layers or for passive insulation/electrical conducting and packaging in a device fabrication. We then discuss plasma-based thin film removal techniques and setups for pattern transferring. The benefits of different hardware configurations and how to choose the correct hardware to suit some particular applications will be highlighted. Selected case studies from magnetic memory/storage device fabrication will be presented to show how to tune the thin film process window to obtain optimized final device performance. Such magnetic device fabrication involves

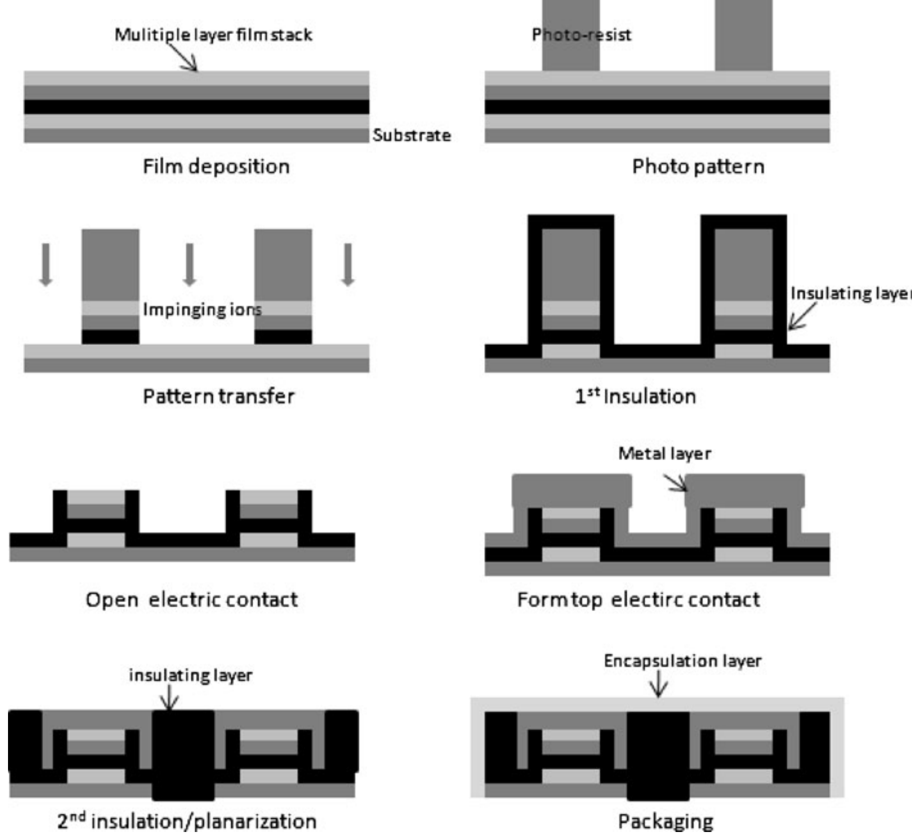


Fig. 1 Typical thin film nano-device fabrication process flow

challenging process control, such as layer thickness tolerances in the range of a few angstroms, device dimensions of ~20 nm, with etching chemistry and byproducts which are non-volatile and sometimes, corrosive.

Vacuum aspects

Why we need a vacuum

Due to the significant advancement of vacuum science and technology in the last half century, ultra high vacuum (UHV) generation and measurement techniques have been widely used in micro-electronics and other thin film based nano-device fabrications. This is largely driven by the stringent impurity control requirement for modern nano-devices. For example in both giant magneto-resistive (GMR) and tunneling magneto-resistive (TMR) devices for information storage applications, the synthetic anti-ferromagnetic coupling is achieved with an ultra thin (~9 Å) Ru layer sandwiched by two magnetic layers [1]; while a tunneling barrier with a thickness of ~7 Å is very common, to achieve a resistance × area product (RA) of <1 Ω μm^2 for a storage capacity approaching 1 Tb/in^2. The process challenging to control such thin layers at the atomic level is enormous. To enable a good thickness control for these critical layers, it is essential to lower the deposition rate to about ~0.1 Å/s, so that there is sufficient time to deposit a layer of a few angstroms and minimize the wafer to wafer thickness variation. However, as the film deposition rate is reduced to close to the background impurity impingement rate, film quality control is vital. We need to either increase the film growth rate (at the price of losing thickness control) or reduce the background impurity level using an UHV system.

As shown in Table 1, the time required to form a monolayer (1 monolayer = 10^{15} molecules/cm^2) of impurity can be dramatically increased under UHV (the calculation here is based on nitrogen gas and assumes a sticking coefficient equal to 1). UHV is evidently essential where critical layer thickness approaches atomic levels.

Figure 2 shows another example highlighting the background moisture/oxygen impact on a thin film specular stack with the following structure:

Ta/NiFe/CoFe/Al + oxidation/Ta cap.

Table 1 Calculated time to form a ML of impurity on substrate at various vacuum levels

Pressure (Torr)	Gas impingement flux (cm^2 s)	Time to form a gas monolayer
760	3.2×10^{23}	3.1×10^{-9} s
10^{-7}	4.2×10^{13}	24 s
10^{-11}	4.2×10^{9}	2.4×10^{5} s (~2.8 days)

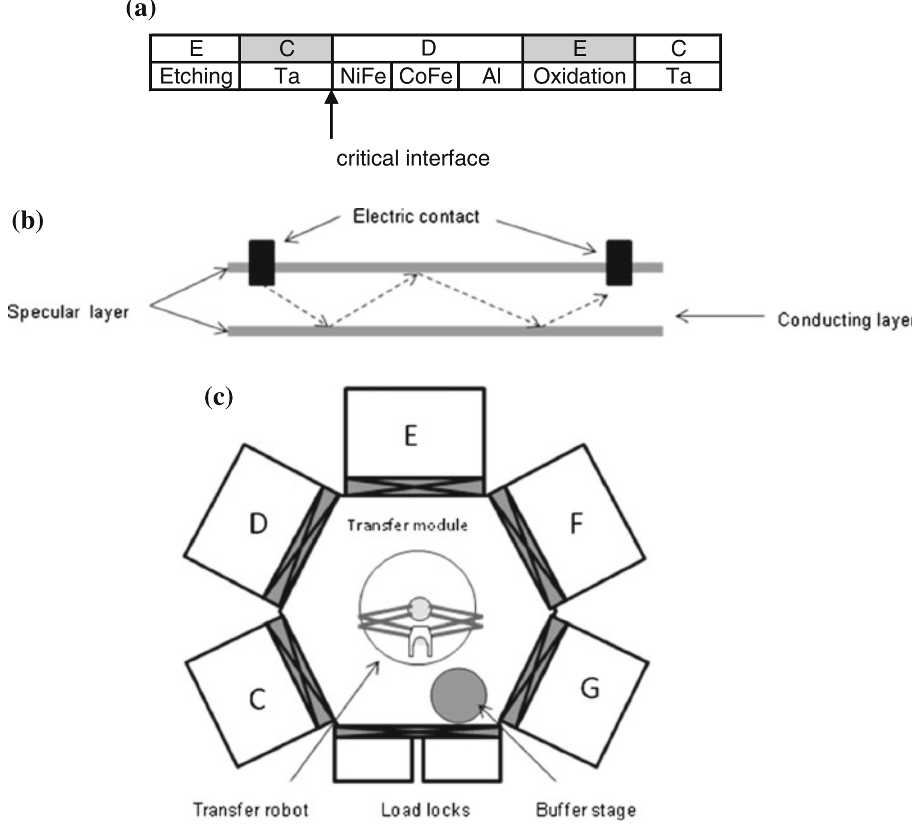


Fig. 2 Schematic drawings showing (**a**) a specular stack, (**b**) working principles of specular structure, and (**c**) the cluster tools used to make such specular stack

The Ta and NiFe interface here is very critical in such a stack as it affects the NiFe/CoFe film growth on top of it and thus the corresponding sheet resistance. Such a specular film stack layer has been used to define the barrier oxidation time in TMR devices [1]. All films are deposited in a multiple chamber cluster PVD tool as shown in Fig. 2c. E is the etching chamber equipped with RF biasing for wafer surface contamination/moisture removal. C and D are PVD sputtering chambers, Ta is installed in chamber C and NiFe, CoFe, and Al are installed in chamber D. To complete the above specular stack, wafer transfer between chambers is required in such a cluster tool.

After cleaning in chamber E, the absorbed surface moisture on the wafer surface desorbs and releases to the transfer module through the gate valve between E and the transfer module. Residual gas analysis (RGA) results shown in Fig. 3 clearly show that the water moisture level in the transfer module increases as the slit valve opens and closes between chamber E and the transfer chamber, indicating that such a moisture level in the transfer module will gradually build-up with the increase of processed wafer numbers in chamber E. More than 12 h baking is normally required once the transfer module moisture level reaches a certain level or when the module is opened for maintenance. In a film stack requiring wafer transfer between PVD chambers and transfer module, the probability of moisture contamination on a freshly grown film increases as the transfer time increases. When the cluster tool runs wafers in a cascading process mode (i.e., where there are multiple wafers within the cluster tool at the same time for higher throughput), the second wafer needs to wait in the transfer module until the first wafer is moved out from a process chamber which the second wafer needs to visit. As a result, different wafers have different waiting times in the transfer module. The sheet resistance of the

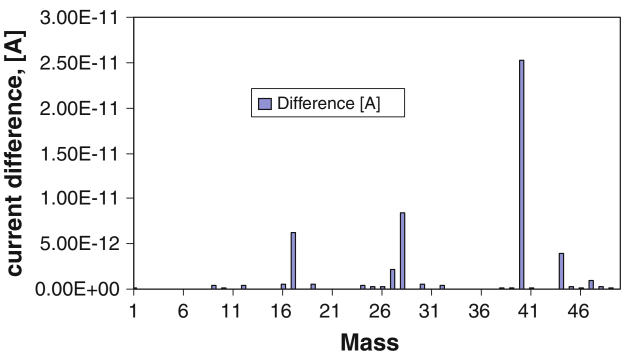


Fig. 3 Transfer chamber RGA current change after etching chamber gate valve close/open operation. Peaks with mass 17(OH), 28(N_2), 40(Ar), and 44(CO_2) are evident

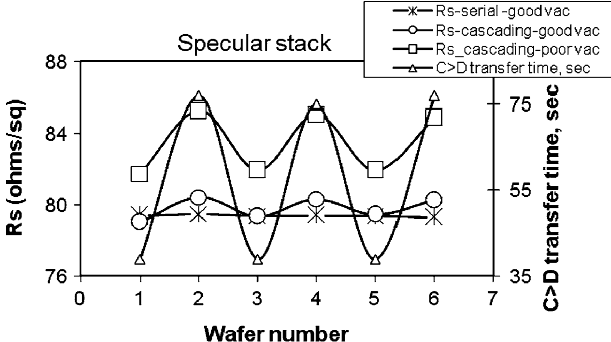


Fig. 4 (*Right Y*-axis) Chamber C to chamber D transferring time of odd/even wafers during the specular stack process when run in cascading mode (multiple wafers in the process tool at one time). (*Left Y*-axis) The resulting sheet resistance variation due to the difference of such transferring time and the impact of background base vacuum. *Note*: good vacuum $\sim 10^{-9}$ Torr (with 12 h chamber baking of transfer mode); poor vacuum $\sim 10^{-8}$ Torr base pressure (without baking the transfer mode) [1]

specular stack above shows a clear wafer to wafer oscillation pattern (see Fig. 4). Those wafers waiting longer in the transfer module after Ta deposition (exposing the critical interface to moisture attack) show higher sheet resistance. When the cluster tool runs in a single wafer mode, i.e., only one wafer in the whole cluster tool all the time and the second wafer enters only after the first wafer has finished all layer depositions, such wafer to wafer sheet resistance oscillation disappears. The data from Fig. 4 confirms further that a better base vacuum in the transfer module enables lower sheet resistance and oscillating amplitude due to the lower impurity levels [1].

There are many other critical films which are very sensitive to water moisture or oxygen exposure, such as Mg (used for MgO tunneling barriers) and iron (or iron-rich $CoFe_x$ used for magnetic layers). Figure 5 shows the corrosion spots of Mg and delamination marks of iron film after exposure to the ambient environment for 2 weeks.

UHV is clearly a requirement for nano-scale thin film processes.

Vacuum generation

Various methods have been employed to generate vacuum with different base pressures. Basically, vacuum is created by removing gas molecules from a vacuum vessel, either via mechanical evacuation or by absorption (physical or chemical). The mechanical pumps include dry roughening and turbo-molecular pumps.

Modern roughening dry pumps usually run hot and do not contain any cooling liquid, and are designed to handle corrosive gases. Such hot operation of a dry pump prevents the condensation of process gases or byproducts from etching and the plasma enhanced chemical vapor deposition (PECVD) process. Frequently, a gas purge may be further employed to avoid condensation of process byproducts within the dry pump.

A turbo pump is essentially an axial flow compressor consisting of many rotor–stator pairs or stages mounted in series. Gas captured by the upper stages is transferred to lower stages where it is successively compressed to the level of the fore-line vacuum pressure.

Absorption pumps include physical absorption pumps, such as the cryo-pump and chemical absorption pumps, such as the titanium sublimation pump and ion pump. Physical absorption pumps capture and remove the gas molecules via their condensation on a cold surface. Chemical absorption pumps capture and remove/bury the gas molecules through chemical reaction and formation of non-volatile byproducts.

Process conditions (gas chemistry, flow rate, etc.), background impurity requirements, and the cost (capital cost and tool down time, etc.) will largely govern the choice of the vacuum generation pumps. For instance, for the same cryo-pump, different designs could have very different performance. Figure 6 shows the maximum amount of Ar that can be absorbed before potential outgassing occurs for three types of pumps. Obviously, pump 1 outperforms the other two types.

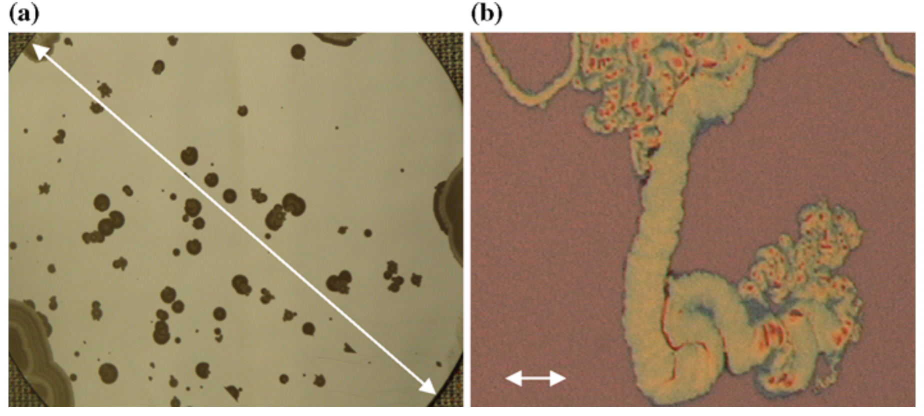


Fig. 5 (**a**) Appearance of a 200 Å thick Mg layer deposited on Si wafer after exposed to atmosphere for 2 weeks. The corrosion *spots* from edge and center of wafers are clearly visible. *Arrow* = 150 mm. (**b**) Appearance of a 70 Å thick iron film deposited on Si wafer after exposed to atmosphere for 2 weeks. The corrosion *spots* and delamination are clearly visible. Magnification *scale bar* = 50 µm

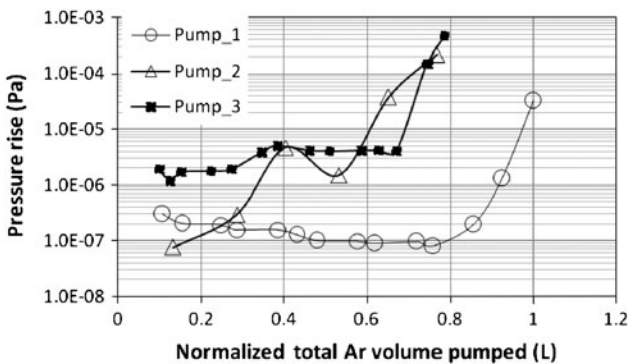


Fig. 6 Pressure rise as a function of total pumped Ar volume for three types of cryo pumps. Pressure was measured after Ar had stopped flowing for 10 min

Due to the flammability of oxygen, it is not recommended to use a cryo-pump when a process operation requires substantial oxygen content, such as in reactive sputtering and etching. Rather, a turbo pump is a preferred choice in such applications [2].

For UHV industrial thin film processes, a turbo pump backed by an oil-free dry pump is usually used for processes containing reactive/corrosive species, such as oxygen, hydrogen, F, Cl, and NH_3; while a cryo-pump backed by an oil-free dry pump is the primary choice for processes using inert gases such as Ar, N_2, Kr or Xe (such as in sputtering deposition).

In addition to the use of conventional high vacuum pumps (cryo pumps and turbo pumps), getter-materials, such as Ta or Ti, Ba, etc. are sometimes deposited in situ to reduce the moisture and oxygen level further in a sputtering system [3] as a temporary method to boost the vacuum.

Plasmas

What is plasma and why we need plasma

Plasma is a fourth state of matter distinct from a solid, liquid or gas. It is a quasi neutral gas of charged and neutral particles which exhibit collective behavior [4]. Plasmas can be generated by applying an electric field across two electrodes in a vacuum vessel containing gases at reduced pressure.

If there is no appreciable electric field across the plasma, ions and electrons tend to drift to the wall by diffusion and are lost when they hit the wall via recombination. Since electrons have much higher thermal drift velocities than ions, they are lost faster and the plasma as a result is not charge balanced, instead it has a net positive charge. The plasma must then have positive potential with respect to the wall to counterbalance the faster electron loss. However, such a positive potential cannot be distributed over the entire plasma, since Debye shielding will confine the potential variation to a layer of the order of several Debye lengths in thickness (or a few hundred micrometers at 1 eV and 10^{10}/cm^3 electron density from Eq. 1). This layer, which must exist on all cold walls, with which the plasma is in contact, is called the "sheath" which contains the plasma.

$$\lambda_D = \sqrt{\frac{kT_e \varepsilon_0}{n_e e^2}} \approx 743\sqrt{\frac{kT_e(\text{eV})}{n_e(\text{cm}^{-3})}}(\text{cm}) \tag{1}$$

where T_e is the electron temperature, n_e is the electron density in plasma.

The function of this sheath is to form a potential barrier so that the more mobile electrons are confined electrostatically.

Due to their low mass, electrons gain energy much more rapidly than ions from the external electric field, E.

$$W = \frac{(E \times e \times t)^2}{2m} = \frac{3}{2}kT \tag{2}$$

where W is the energy gained or worked done by external electric field for the charged particles after time t. m *is* the mass of an electron or an ion, respectively; T is the respective electron or ion temperature (i.e., T_e or T_i).

At low pressure, the collision probability between electrons and neutrals is too small to achieve thermal equilibrium. So electrons have higher energy ("hot", or higher T_e) than ions and background gas molecules, i.e., $T_e \gg T_i \gg T_g$. Such hot electrons (1 eV is equivalent to 11,600 K from Eq. 2) can create energetic species (ions, excited species-radicals, etc.), which are more reactive compared with ground state molecules or neutrals. As a result, a plasma can significant enhance the chemical/physical reactions, which usually require high temperatures. This is particularly useful for thin film processes on temperature sensitive substrates, which cannot withstand high thermal load.

How to generate a plasma

Plasma can be created in two ways: with heat or by energizing electrons. While energetic electrons can be created by DC, RF or pulsed power or electron cyclotron resonance (ECR) electro-magnetic fields.

Important plasma parameters

Figure 7 shows schematically the three distinguishable regions in a plasma generated between two electrodes, separated by a distance, namely, sheath regions (cathode and anode), bulk plasma region, and surface region (wafer surface on cathode electrode), respectively.

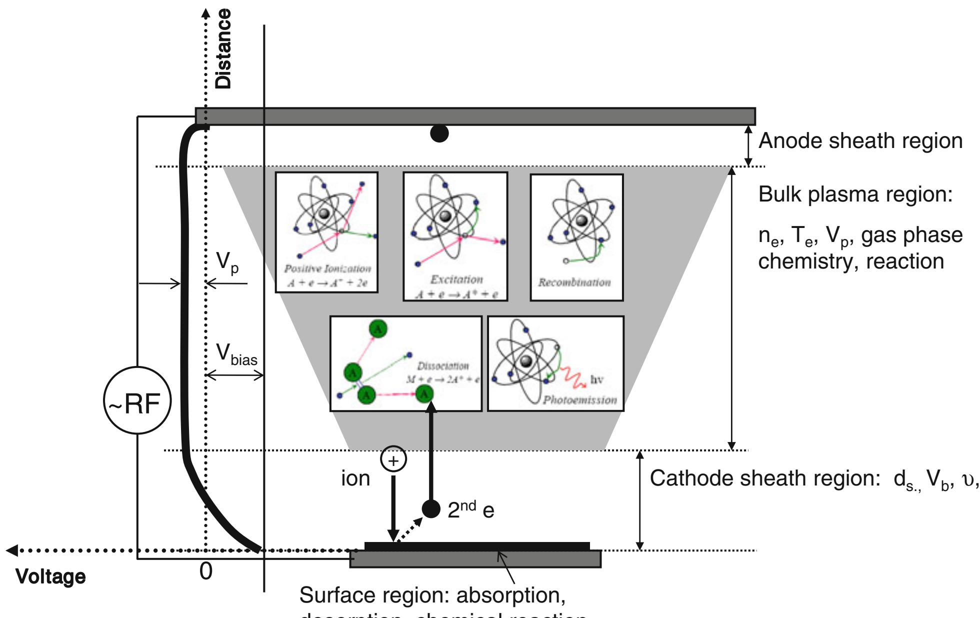


Fig. 7 Important plasma regions

The Bulk region involves plasma properties, such as the electron density (n_e) by Eq. 3; electron temperature (T_e) by Eq. 4; plasma potential (V_p); and plasma frequency (for both ions and electrons) (f) by Eqs. 5–7; and electron-neutral collision frequency (v) by Eq. 8;

$$\overline{P} = \frac{\text{Power}}{\text{Volume}} = J \times E = \mu E^2 \tag{3}$$

$$\frac{E}{P} \propto \frac{E}{N_g} \propto \frac{E}{v_c} \propto T_e \tag{4}$$

$$f_{\text{electron}} \approx 9000\sqrt{n_e}\text{Hz} \tag{5}$$

$$f_{\text{ion}} \approx f_{\text{electron}}\sqrt{\frac{m_{\text{electron}}}{m_{\text{ion}}}}\text{Hz} \tag{6}$$

$$f_{\text{gryo}} \approx 2.8B_0\text{MHz} \tag{7}$$

$$v_{\text{electron-neutral}} = N_g V_e \sigma \approx 2\,\text{MHz/mTorr} \tag{8}$$

where J is current density, E is electric field, μ is the conductivity, n_e is electron density in cm^{-3}. f is the frequency. B_0 is the external magnetic field. N_g is gas density, V_e is the electron kinetic energy, and σ is the collision cross-section between electrons and the neutrals.

It is important to understand the above frequencies associated with a plasma source. For example, if the external electromagnetic wave frequency $f_{\text{external}} > f_{\text{electron}}$, it will be transmitted through the plasma; if $f_{\text{external}} < f_{\text{electron}}$, it will be reflected.

In addition to the active species (ions, radicals, high energy neutrals, photons, electrons) concentrations, their lifetime and residence time in a plasma system are also critical, particularly for plasma-based etching process.

In the *sheath region*, there are a few key parameters, such as (1) sheath thickness (d_s); (2) cathode sheath fall (V_b), which determines the ion energy across the cathode sheath ($E_{\text{ion}} = e(V_p$ (plasma potential) + V_b (bias)), for a collision-less sheath); (3) collision frequency between ion–neutral–radical, v.

The Surface region is critical in determining the absorption, desorption, and chemical reactions.

Table 2 gives further details of the characteristics of bulk and sheath regions in a plasma source.

Plasma sources

Most low and medium density plasma reactors are capacitively coupled while high density plasma (HDP) sources are generated by inductively coupled RF, microwave, surface wave, ECR, and capacitively coupled ultra high frequency (UHF) RF. Such HDP sources are primary used for PECVD and etching. For thin film deposition, conventional DC or RF (13.56 MHz) plasma sources are still widely used. It is beneficial to understand the energy transfer (or heating) mechanisms for various plasma sources and their pros and cons, as highlighted in the following sub-sections.

Capacitively coupled plasma (CCP) source In a CCP source, the majority of the external energy from

Table 2 Important characteristics and features of the sheath and bulk plasma regions

	Bulk plasma	Sheath region
Electrons	Electron density (N_e)	Less electrons than ions
	Electron energy (T_e)	
	Electron energy distribution function (EEDF)	
	Plasma potential (V_p)	
Ions	Generally, $N_e = N_i$	Bias voltage (V_b)
	$T_i \ll T_e$	Plasma potential
	Ion responds to electric field much slower than electron	Ion flux (J_i)
		Ion energy ($V_b + V_p$)
		Ion energy distribution function (IEDF)
Radicals	Plasma chemistry	Concentration on substrate surface
	Species types	Etching
	Species concentration	Deposition
	Lifetime	
Neutrals	Background gas	Background gas
	Affect the recombination of electron-ion pair	Affect the ion energy impinging the substrate
	Affect the recombination of radicals and radical with neutrals	Affect the reactive species interacting with substrate
		Affect the diffusion of byproducts from substrate

electromagnetic field is dissipated across the sheath regions via the ion bombardment of the electrodes (P_{ion}) and the secondary electron generation (accelerated towards the bulk plasma for further ionization $-P_{\text{electron}}$). Increasing the input power will increase the ion/electron density in the plasma (Eq. 3), however, since most of the external energy is dissipated across the sheath, the sheath voltage will increase too, and this results in strong ion bombardment of the electrodes and the wafers placed on top of them (primarily for etching). Device damage is a concern. For sputter deposition, this is less of an issue if the wafer is placed on a grounded stage, further away from the plasma source (target surface); but high energy neutrals still pose a damage risk during thin film growth.

Ohmic heating is dominant in lower frequency CCP reactors. Energy is transferred into the plasma through electron-neutral particle collisions. Such energy transfer efficiency is at maximum when the collision frequency equals the RF power driving frequency, i.e.

$$v_{\text{e-N}} = f_{\text{rf}} \tag{9}$$

At very low pressure, the electron-neutral collision probability is drastically reduced. Fortunately, stochastic heating becomes dominant then, i.e., electric energy is transferred into the plasma via electron reflection from a very fast moving sheath surface. The energy transfer efficiency in this mode does not depend on neutral gas pressure and increases with increasing RF frequency, f_{rf}. That is why 60 MHz driving frequency or higher is used in most modern high density PECVD systems, like the SiN process discussed later. However, careful matching network design is more critical for UHF source as the skin depth becomes very thin and RF leakage control is more challenging.

Inductive coupled plasma (ICP) source In an ICP source, the external electromagnetic energy transfer process could undergo various stages, depending on the RF power level and presence or not of an external magnetic field, B.

During the ignition of the ICP source, the large reactive energy component (for a high Q matching circuit in particular, when a Faraday shield is used) stored within inductor will generate a sufficiently high E_z field (along the solenoid center line direction) across the RF coil (Eq. 10) [5] (see Fig. 8). Such a high E_z field will initiate conventional breakdown.

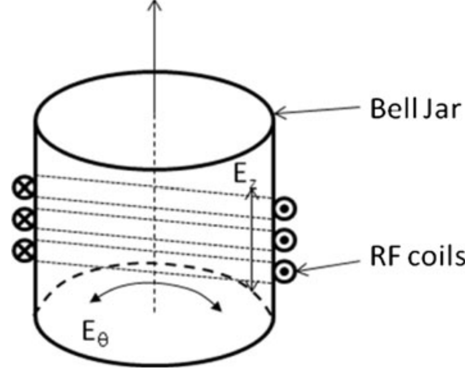


Fig. 8 Electrical field during the plasma ignition in an ICP system

$$E_z = \frac{|V_{coil}|}{d} = \frac{2\pi f L_{coil}|I_{rf}|}{d} \quad (10)$$

where d is the RF coil length and f is the RF frequency, L_{coil} is the inductance and I_{rf} the RF current.

After plasma ignition and the time-varying RF current flowing into the RF coil starts to generate a time-varying magnetic field, B_z, which then creates another time-dependent azimuth electric field, E_θ, which wraps around the axis of the solenoid/bell jar (Eq. 11). This azimuth electric field, E_θ, then induces a circumferential current in the plasma and accelerates electrons to gain energy, creating enough energetic electrons to initiate further ionization and sustain the plasma.

$$E_\theta = \frac{2B_z\pi^2 r^2 f}{2\pi r} = \mu_0 rfNI_{rf} \quad (11)$$

where N is the number of coil turns, d is the coil length, and r is the coil radius, I_{rf} is RF current, f is the frequency of the RF source.

Depending on the configuration (with or without the magnetic field) and the applied power level, an ICP source can transit from one mode to another.

- At low power ($n_e < 10^9$ cm^{-3}), the plasma conductivity is low and the classical skin depth is large. There is little shielding of electromagnetic fields and capacitive coupling from the antenna is dominant (E-mode).
- As the skin depth decreases in the plasma source with increasing electron density, the plasma produced currents shield the imposed electromagnetic field, resulting in inductive coupling (H-mode) [5].
- If there is an axial static external magnetic field, the external electromagnetic energy can penetrate into the core of the plasma and couple to the helicon wave (W-mode) [6, 7].

Due to the above-mentioned different heating mechanisms, CCP sources behave differently compared with ICP sources. In the plot shown in Fig. 9, the plasma system is powered with two RF power supplies: one is capacitively coupled to the wafer stage; another is connected to the Al_2O_3 bell jar via copper coils (ICP mode) above the wafer stage. Both RF power sources are driven at a frequency of 13.5 MHz. The system can be thus operated in either ICP, or CCP (or ICP + CCP) mode.

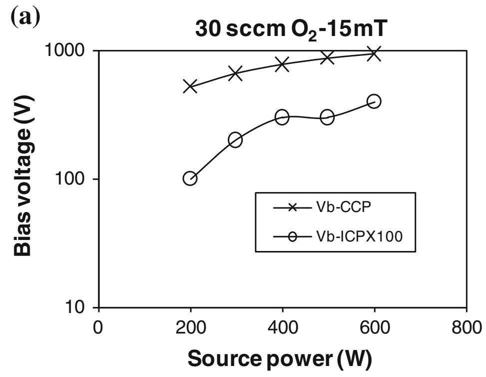
Results from Fig. 9 clearly demonstrate the difference between CCP and ICP sources for a pure oxygen discharge at 15 mTorr in terms of bias voltage and electron/ion density (proportional to the dissociation extent of O_2). The ICP source has a lower wafer stage bias (plasma floating potential ~ a few tens of volts—note the scale is multiplied by 100 in the plot). In the CCP mode, the bias jumps up quickly with the increase of RF power as we discussed earlier. The O_2 emission intensity from the ICP mode is much larger than the CCP mode, indicating more effective external electric energy transfer to the plasma in ICP mode. In other words, electric energy is pumped to the plasma mostly for gas phase ionization in the ICP mode; while it is consumed across the sheath in the CCP mode.

To achieve a HDP, we need to suppress the ion energy component dissipated across the plasma sheath, whilst increasing the electron energy component transferred to the bulk plasma for ionization, i.e., reducing the $P_{ion}/P_{electron}$. In this way, more energy will go to electron generation within the bulk plasma, rather than be dissipated within the sheath regions to generate heat. It has been found that such $P_{ion}/P_{electron}$ ratios can be approximately described in terms of RF current (I_{rf}), chamber pressure (p), and RF source frequency (f) by Eq. 12 [8–11].

$$\frac{P_{ion}}{P_{electron}} \propto \frac{I_{rf}}{pf^2} \quad (12)$$

Also, minimizing the electron loss via adequate electron trapping mechanisms, such as by utilizing a magnetic field gradient, is also helpful to maintain a higher electron density in the plasma.

Other HDP sources ICP, CCP, and ICP + CCP sources are commonly used in thin film deposition and etching. Due to their plasma density limitation, other HDP sources have been actively developed in recent years for large scale



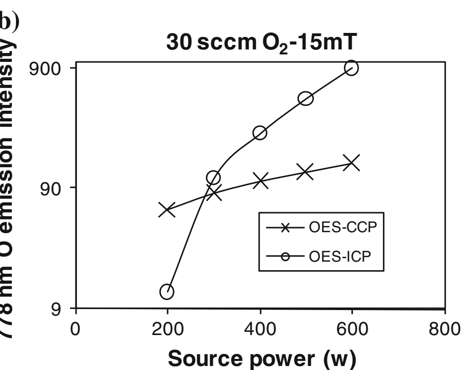


Fig. 9 (**a**) Substrate bias voltage and (**b**) the oxygen emission intensity at 778 nm as a function of the source power for 15 mTorr O_2 discharge from an inductive coupled plasma (ICP) and capacitive coupled plasma (CCP) source, respectively

Table 3 Comparison of various plasma sources

Plasma source	Operation pressure (Pa)	Electron temp (eV)	Plasma density (#/cm^3)	External B field (G)	System complexity	Uniformity
CCP	2–10	4–7	$\sim 10^{10}$	NO	Low	Good
ICP	1–3	3–5	10^{10}–10^{11}	NO	Low	Very good
ECR	0.05–2	5–10	10^{10}–10^{13}	875	Complex	Not very good
NLD	0.1–1/0.5–4	2–3	10^{10}–10^{12}	5	Slightly complex	Excellent
Helicon	1–10	n/a	10^{12}–10^{13}	10–300	Very complex	Few data

CCP capacitively coupled plasma, *ICP* inductively coupled plasma, *ECR* electron cyclotron resonance, *NLD* neutral loop discharge

industrial usage. These HDP sources include: (1) UHF (>60 MHz) CCP sources [9, 12–14], (2) ECR sources with the application of a ~875 G external magnetic field [15–20], (3) neutral loop discharge (NLD) plasma source [18, 19], and (4) helicon plasma source (with application of 10–300 G external magnetic field) [20].

Table 3 compares the achievable plasma density and electron temperatures for various plasma sources and their complexity.

(1) UHF CCP

For conventional 13.56 MHz RF CCP, with increased discharge power (or current), most of the energy will be dissipated across the sheath, without generating ionization within the bulk plasma. However, for much higher than 13.56 MHz frequencies, plasma inductance may be significant, such that the sheath effect as a capacitance may be reduced and this enables an increased power absorption in the bulk plasma and thus increases plasma density [12]. As ions and electrons can be trapped in the plasma at UHF more effectively, a stable plasma with high electron density can be sustained with lower electron temperatures and low plasma potentials [13, 14]. Such a UHF plasma source has been widely used for "damage-free" critical thin film formation, such as in a-Si:H solar cells and other microelectronic devices.

(2) Microwave and ECR sources

As the collision frequency between electrons and neutrals is close to one GHz at pressures in the Torr range, collisional heating for a plasma source driven at 2.45 GHz frequency is the primary energy absorption process, while a magnetic field has little impact on the heating of the electrons at such a high pressure. However, when pressure goes from the Torr to below the mTorr range, the electron-neutral collision frequency drops proportionally from the GHz range to MHz, i.e., much less than the microwave driving frequency. As a result, high MW power is necessary to sustain the plasma if no external magnetic field is applied. Fortunately, with an external magnetic field of 875 G, electron gyro-frequency is equal to the microwave driving frequency at 2.45 GHz and electrons can be accelerated constantly to much higher energy and enable the ionization of background neutrals.

The external magnetic field for an ECR plasma at microwave frequency is very large and requires sophisticated hardware engineering to obtain uniform plasma density across large substrate areas and suffers from higher cost and system complexity.

(3) NLD plasma source

Recently, a new source called the NLD system has been developed, which only requires ~5 G of external magnetic field while still maintaining a sort of ECR effect at 13.56 MHz, which is much easier to deal with in terms of shielding and energy transfer handling compared with microwave frequency. Plasma density up to 10^{12}/cm^2 has been reported with very low electron temperature, which is attractive for dedicated material processing sensitive to damage caused by high energy electrons [21].

(4) Helicon source

The helicon source differs from conventional ICP plasmas in that a magnetic field B_0 (10–300 G) is required to launch a helicon wave. Once the gas in a processing chamber has been weakly ionized by the electrostatic voltage on the antenna, the application of B_0 causes the antenna to launch circularly polarized helicon waves; the wave energy is subsequently converted to electron energy, thus raising the degree of ionization. Although high plasma densities up to 10^{13}/cm^2 can be achieved with a much lower magnetic field compared to ECR [20], the helicon source is less commonly used commercially due to its complexity and unclear cost/performance benefit over the inductively coupled plasma source. Nevertheless, there is a helicon sputtering source on the market as shown in Fig. 10.

Contamination caused by the CCP component

Although the wafer is subjected to much lower bias voltage in a pure ICP source, the coil voltage is still very high

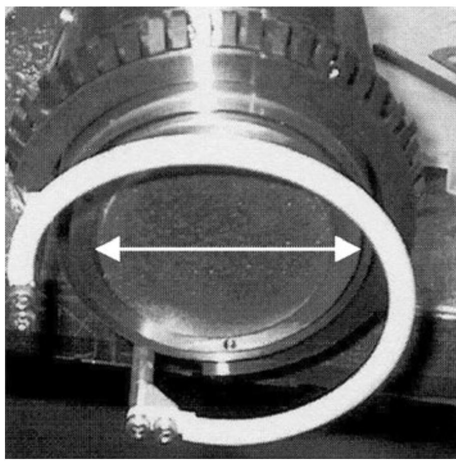


Fig. 10 A helicon coil used to enhance low pressure magnetron sputtering for ultra low deposition rate. The magnetic field, B_0 required for wave mode is provided by the magnetron itself. *Arrow* = 30 mm

during plasma ignition, which alternately acts between the coil and grounded substrate/top plate. After breaking down, the high energy particles are accelerated by the RF field and bombard the substrate, top plate, and the ceramic insulator wall. This can cause substantial erosion from the substrate stage, top plate, and the quartz/Al_2O_3 ceramic bell jar [22].

Figure 11 clearly shows erosion marks on an alumina bell jar used in an ICP etching reactor. The lighter spots adjacent to the PTFE coil positioning blocks are clearly visible. This could be due to the higher dielectric constant of PTFE ($\varepsilon_r = 2.2$) compared to the air gap ($\varepsilon_r \sim 1$) where there is no PTFE. The PTFE enhances the impinging electric field due to charge polarization, which occurs in dielectrics.

Faraday shield to filter CCP component

Capacitive coupling components in non-shielded sources increase the sheath potential adjacent to the coil, causing ion bombardment at that part of the wall, as seen from

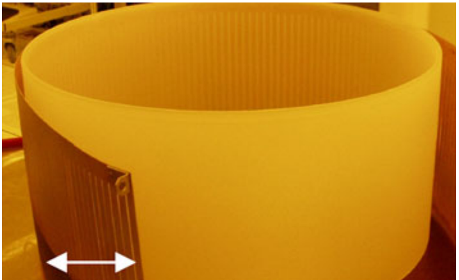


Fig. 12 Faraday shield around a quartz bell jar. *Arrow* = 60 mm

Fig. 11. Such sputtering and etching lead to non-uniform wall conditions and vessel erosion, particularly during reactive etching with Cl and F species. To minimize such erosion, electrostatic shielding (Faraday shielding) is usually applied to filter out the undesired CCP component from the ICP source (see Fig. 12). However, a high Q value start-up circuit is required to ignite the plasma at the first instance when the CCP component is effectively removed [22].

Dual frequency plasma source

A plasma source with a well-separated plasma-generation zone and an independent ion energy control is particularly attractive for device patterning and etching. Ideally, the plasma source zone is solely used to generate the desired electron/ion density (active species concentration), while the biasing region is used to control the ion energy without sacrificing the active species distribution uniformity.

A dual frequency plasma source is designed to achieve this goal by keeping the biasing electrode driving frequency lower; whilst keeping the source plasma density high [23], so that the CCP biasing electromagnetic (EM) wave driving frequency f_{ccp} is very much less than the plasma frequency in the source f_{pe} (Eq. 5). The biasing EM field should be reflected by the plasma source and not cause any absorption.

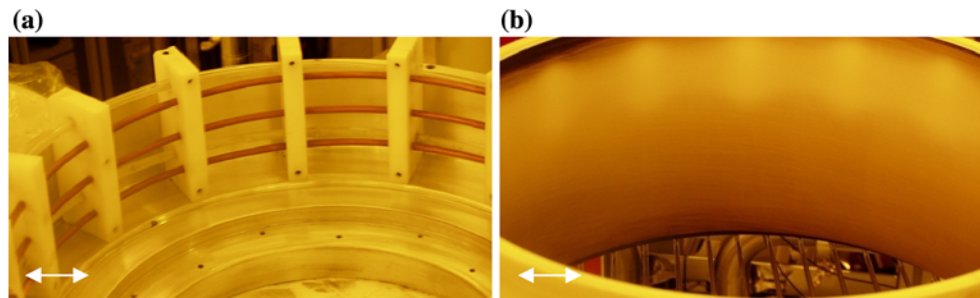


Fig. 11 Copper RF coils and their supporting PTFE blocks (**a**), and the alumina bell jar erosion marks in contact with plasma source (**b**). *Arrow* = 30 mm

Plasma-based thin film deposition process

Thin films can be deposited by various methods, including (1) thermal processes (evaporation, laser ablation, and plasma spraying—primary for thick coatings), (2) electroplating from solution, and (3) vacuum plasma-based processes (physical vapor deposition (PVD), plasma enhanced CVD (PECVD), and ion beam deposition (IBD)). Here we focus on the last category.

Magnetron sputtering

Magnetron sputtering is one of most commonly used PVD methods. To control the film properties, it is important to understand a few important parameters, such as the trajectories of sputtered atoms from the target surface and the momentum transfer influencing sputtering yield. This is particularly critical to control the film composition in a compound target.

Igniting and sustaining plasmas at low pressure

To better control the film growth, lower pressure magnetron sputtering is usually required, which makes the plasma ignition difficult as the gas breakdown is governed by Paschen's law, i.e., $p \times d =$ constant, where p is the pressure and d is the distance between the electrode gap where a high voltage is applied. The constant varies and depends on the types of gases used in a discharge and the electrode materials.

This dilemma is easily solved in modern sputtering tools via the gas triggering mechanism, i.e., a high flow rate gas pulse is introduced into the sputtering chamber for a short time to bring up the pressure to the breakdown point, just before the plasma ignition. After that, gas flow is reduced to normal operation level as shown in Fig. 13. Clearly, a 2 s gas pulsing at 200 sccm easily brings up the pressure to 6 mTorr, high enough to ignite the plasma and such pressure quickly decays to the normal operation level of 0.5 mTorr within 3 s after turning off the gas pulse.

However, cautions must be exercised during such triggering. If the gas is introduced locally and if the $p \times d$ approaches the break down point, local arcing may be resulted.

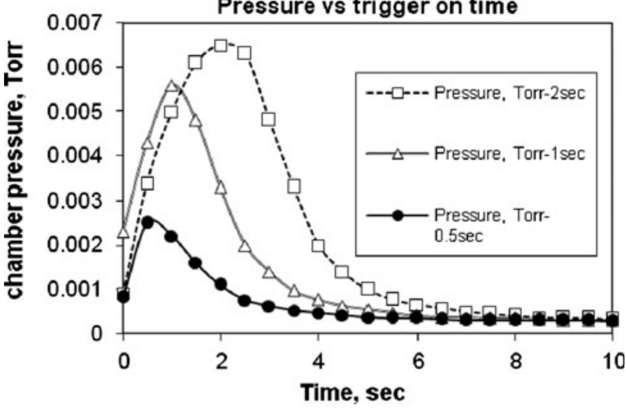


Fig. 13 Chamber pressure as a function of time during gas triggering

Angular distribution of ejected atoms from a target surface

Angular distribution of ejected atoms from a target surface can be largely classified as: (1) over cosine distribution, (2) normal cosine distribution, and (3) under cosine distribution, as shown in Fig. 14. Such distribution patterns depend on the target materials, their crystalline orientations, sputtering gases, and incident beam energy and angle. For magnetron sputtering, the incident ions across the plasma sheath are assumed perpendicular to the target surface. The beam angle effect on such ejected atom's angular distribution is more profound for ion beam deposition (IBD), as discussed in later sections.

If the sputtering gas has similar mass compared with the target atoms, the sputtering gas ions can pass their energy to the target atoms and knock them out and generate film growth on the wafer surface more efficiently (see Table 4). As a result, the film deposition rate will be different for different types of working gases (see Table 5). For instance, Cu, CoFe, and NiFe show high deposition rate using Ar sputtering gas, compared with Kr sputtering gas, as the energy transferring efficiency between Cu/Co/Fe/Ni and Ar is about ~97%, while that between Cu/Co/Fe/Ni and Kr is only about ~75%. However, if the angular distribution shape changes as the sputtering gas varies; the deposition rate also changes and offsets the energy transferring factor effect. For example, if the angular distribution of ejected

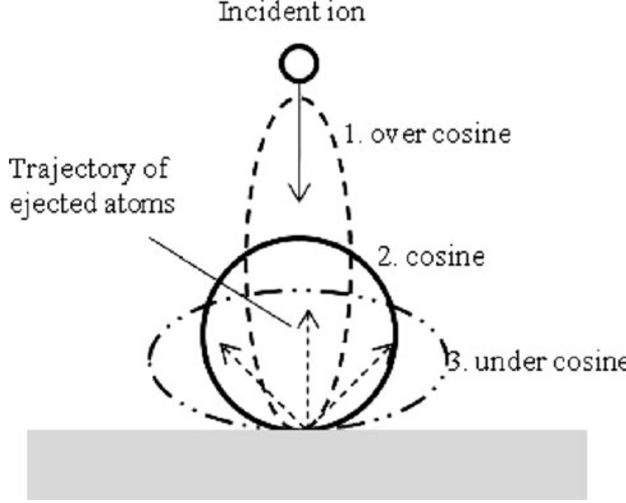


Fig. 14 Trajectory of ejected atoms from a target surface up bombardment from impinging ions

Table 4 Calculated energy transferring efficiency between Ar/Kr gas and various target materials with different masses

Atom	Atomic weight	Atomic #	Energy transferring efficiency using Ar (%)	Energy transferring efficiency using Kr (%)
Pt	195	78	56.50	99.86
Ir	192	77	57.07	99.81
Mn	55	25	97.51	70.70
Ru	101	44	81.28	90.23
Ta	181	73	59.29	99.51
Cu	64	29	94.67	76.31
Ni	59	28	96.32	75.00
Fe	56	26	97.22	72.20
Co	59	27	96.32	73.63
Al	27	13	96.24	46.42

Table 5 The film deposition rate and composition for various sputtering gases

Material	Rate		Pressure (mTorr)	
	Ar	Kr	Ar	Kr
IrMn	0.58	0.43	0.49	0.71
Cu	0.90	0.51	0.34	0.5
$CoFe_{30}$	0.60	0.30	0.27	0.4
Ta	0.54	0.57	0.28	0.42
$NiFe_{12}$	1.20	0.76	0.5	0.75
	At.%, sputtered in Ar		At.%, sputtered in Kr	
Ir	29		23	
Mn	71		77	

Note that the pressure is slightly different from Ar to Kr at the same flow rate, this may be related to the cryo-pump pumping speed difference for these two gases

atoms changes from cosine to under cosine, the atom flux received by the wafer directly underneath the target will be reduced and the actual deposition rate decreases, even though the energy transferring efficiency increases by switching sputtering gas. The IrMn film deposition rate shown in Table 5 is one of these examples.

Operating I–V regions for sputtering

The I–V curve for the sputtering power supply is very useful for monitoring the sputtering process stability. Figure 15a schematically shows how the I–V curve changes during the PVD thin film deposition process. Usually magnetron sputtering is operated within the so called "abnormal" glow region, where the plasma discharge uniformly covers the whole target surface; an increase in the bias voltage will cause an increase in the discharge current (see Fig. 15b).

However, if the operating voltage or current are too low for some ultra low deposition rate process, particularly for thin film heads applications, where the critical film thickness ranges from a few angstroms to a few tens of angstroms, or when there is some soft arcing as particles fall in-between the cathode shield gap, or there is some surface contamination on the target surface, a very unstable discharge with I and V fluctuating may be encounted-as shown by the I–V curve in Fig. 16. The steps on the plot are due to the automatic re-ignition function of the power supply when the discharge is extinguished. Certainly, the film quality prepared under these conditions leads to very poor device performance and precise thickness control is impossible.

Effectiveness of a magnetron

For a magnetron to be effective in trapping electrons for lower pressure ionization, its surface magnetic field should be larger than 300 G [24], regardless of target thickness. The non-uniformity of such a surface magnetic field will affect the target erosion profile. For instance, at the end of the target lifetime, the magnetic field along the target erosion track increases and results in even more non-uniform target erosion. However, the magnetron field should not be too strong either. There is a cut-off magnetic field to provide the benefit of a magnetron, above which the discharge breakdown voltage dramatically drops off. Further increase in the magnetic field results in the increase of breakdown voltage and the plasma extinguishes. When the radius of the circular trajectory of the electrons becomes so small at such high magnetic field, electrons cannot gain sufficient energy from the E field to initiate ionization [25].

The effectiveness of a magnetron to trap electrons can be extrapolated from the I–V discharge curves as shown in Fig. 17 by fitting the current versus voltage using the formula:

$$I = \text{constant} \times V^n \quad (13)$$

where a large n indicates strong electron trapping capability by the magnetic field [24]. The n value is 6 and 13 in

Fig. 15 Current–voltage relation for the various types of plasma discharge between two powered electrodes (**a**) [reproduced from [47] with permission]. Abnormal discharge region for Cu sputtering operated at 0.5 mTorr pressure (**b**)

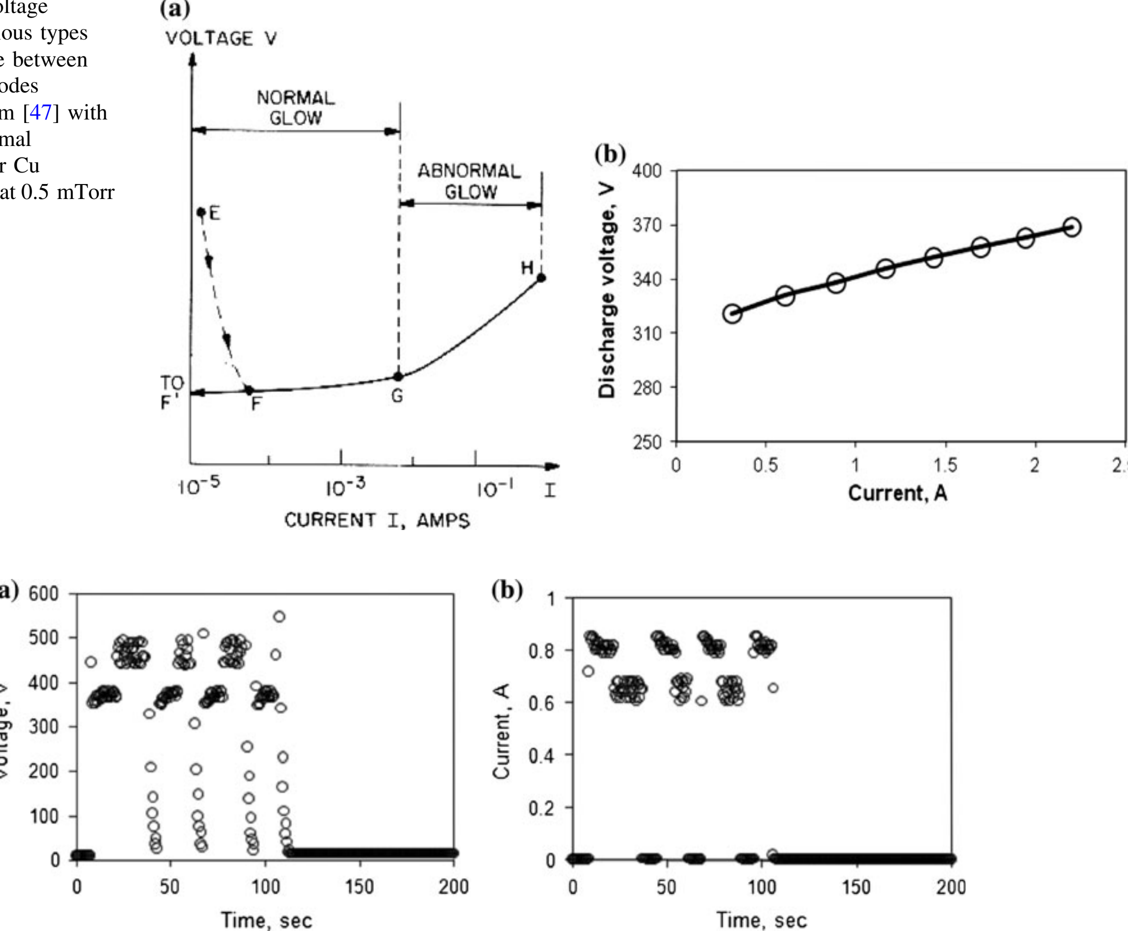


Fig. 16 Unstable discharge I–V curves for a Cu PVD process. (**a**) Voltage and (**b**) current jumps and the plasma eventually extinguishes

Fig. 17 (**a**) I–V curve for Ta deposition with 100 sccm of Ar flow using type #1 magnetron with a surface magnetic field strength of ~700 G and (**b**) Cu with 30 sccm of Ar flow and a stronger type #2 magnetron with a surface magnetic field strength of ~1500 G

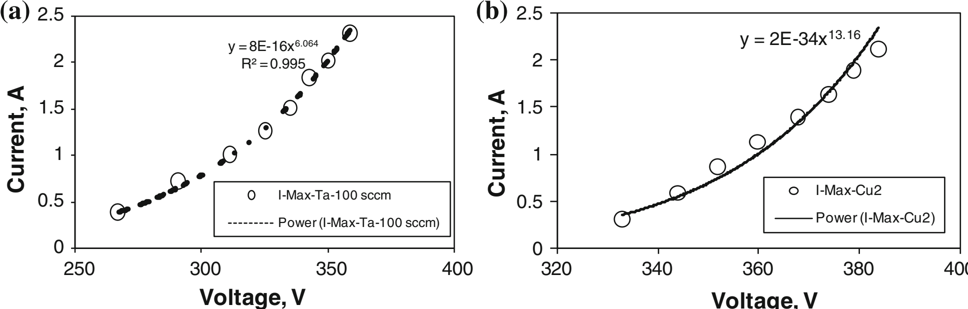


Fig. 17a and b for a magnetron with a surface B field of ~700 and 1500 G, respectively, suggesting that the magnetron in Fig. 17b is more effective in trapping electrons than the magnetron in Fig. 17a.

Caution must be exercised for a magnetic target due to its high permeability. As a result, a significant amount of the B flux concentrates within the magnetic target, rather than leaks out. Therefore, either a thinner target material or a stronger magnetron is required to provide a sufficiently high fringe magnetic field on the target surface for effective electron trapping. Further, the magnetic target material properties can dramatically affect the surface fringe field and thus impact the plasma ignition process. For example, the magnetron's fringe magnetic field leaking out on the CoFe target surface is significantly reduced when its surface layer grain size increased. This makes the plasma ignition difficult when the surface field is reduced below 300 Oe (see Fig. 18).

Fig. 18 Grain size difference for a surface rolled sputter target (sputtering surface on *right hand side* above), *arrow* = 200 μm

Balanced versus unbalanced magnetron sputtering system

Depending on the magnetron design, its fringe field could be closed (by itself or by interacting with the adjacent magnetron's flux lines) or could leak out and reach the wafer surface. Window et al. [26–28] have reported a high ion flux for an "unbalanced" magnetron in which electrons follow "leakage" magnetic flux lines.

Growing film properties on the stage with an aligned magnetic field (largely used for magnetic thin film process) could be further affected by the magnetron leakage field, due to the interaction of stage magnetic field with the fringe field from the magnetron. As a result, the ion bombardment location and intensity will vary as the stage/target magnetic field rotates. Such interaction is shown in Fig. 19. The sheet resistance distribution pattern within wafer for Cu and CoFe varies as the stage magnetic field changes from 0° to 180°, indicating that the impingement ion trajectories affected by the stage alignment magnetic field. Note that the magnetic field on the stage is fixed during this test, but it can be set to rotate during the actual PVD process and can potentially average out this effect.

Substrate biasing effect

The mobility of the atoms arriving at the substrate surface has a strong influence on its microstructure evolution and development. Generally, higher substrate temperatures will result in denser films and larger grain size. However, there are a lot of applications where the substrate cannot tolerate higher temperature. Substrate biasing can effectively

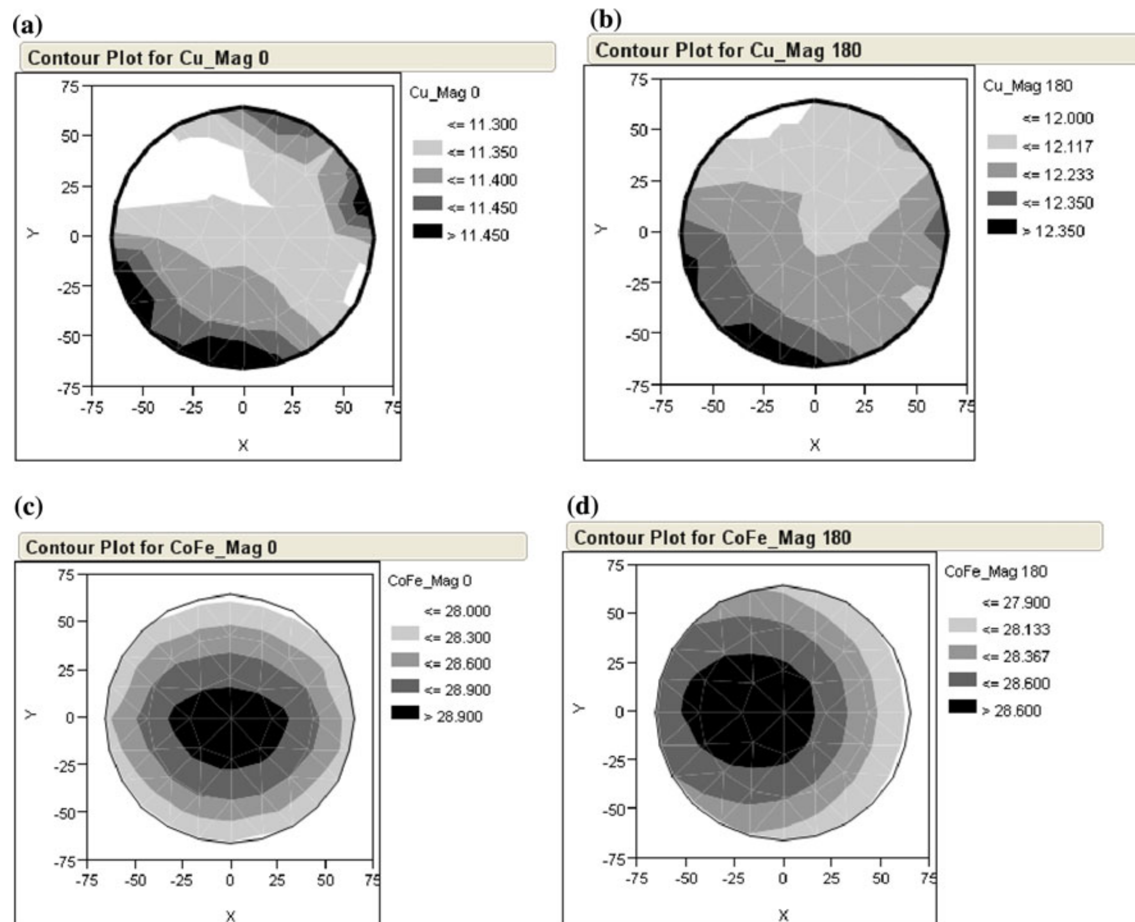


Fig. 19 Sheet resistance distribution changes with various wafer stage magnetic field (~100 Oe) orientation ((**a**) Cu—0°, (**b**) Cu—180°, (**c**) CoFe—0°, (**d**) CoFe—180°) on the film uniformity change for Cu and CoFe films. 0° is defined as N > S is pointing to *Y* direction, 180° as N > S is pointing to −*Y* direction

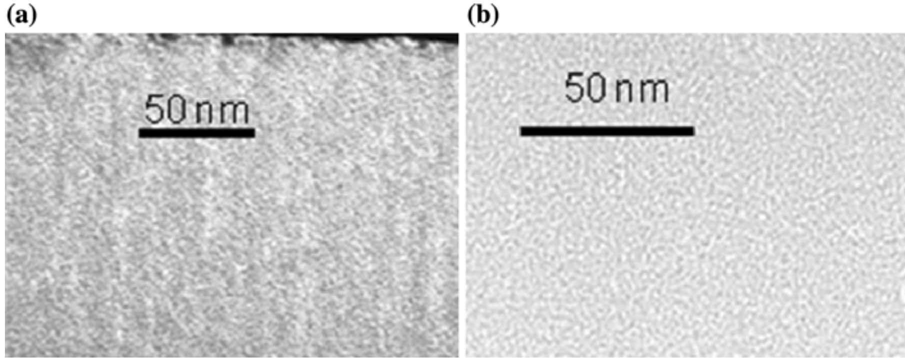


Fig. 20 Amorphous carbon films prepared by PVD sputtering (**a**) without and (**b**) with 100 V negative substrate bias. For those without bias, a columnar structure is visible, while the one with substrate bias is more dense and uniform

increase the adatom's mobility without a large thermal load. That is another reason why plasma enhanced thin film processes are beneficial.

Figure 20b shows that the carbon film is densified when applying a −100 V substrate bias, compared with non-bias film (actually still biased at floating potential ∼−20 V) in Fig. 20a. Such ion bombardment induced film densification has been observed for PECVD SiON film deposited at 325 mTorr before [29] as well in many other film growth systems.

Tilted target versus planar target design

To increase the film uniformity across large substrate surface, the target area needs to be about 1.5–2 times that of a substrate in a typical planar target configuration system, or the target–substrate separation has to be increased (or a collimator may be used). However, increasing the separation for uniformity improvement reduces material utilization as the deposition rate on the substrate drops with the increase of substrate/target separation (see Fig. 21). Fortunately there are still some other ways to tune the film uniformity for the planar target configuration. By tuning

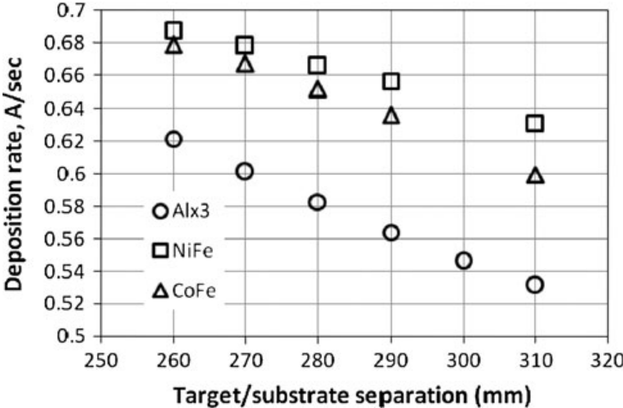


Fig. 21 Deposition rate drops as the increase of target/substrate separation distance for three materials, NiFe, CoFe, and Al. (Ar flow 15 sccm, rotation speed, 60 rpm. Power = 200 W for CoFe/NiFe and 100 W for Al, pressure = 0.5 mTorr)

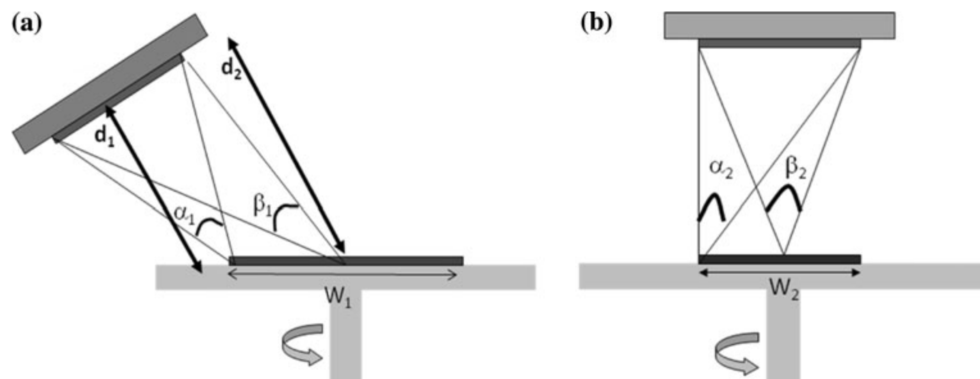
the magnetic field and making the erosion tracks deeper (more or less like a "W" shape), it is possible to make the edge deposition rate higher (see Fig. 22b [30]), to compensate the smaller flux acceptance angle at the wafer edge. Nevertheless, to produce uniform film thicknesses across large substrate areas without increase in cost has significant practical advantages.

The tilted target design shown in Fig. 22a serves this requirement very well. The benefit of this design has been well evidenced from the data shown in Fig. 23. The normalized NiFe film thickness deposited on a stationary substrate has a range over mean of 103%, while this reduces to less than 5% for a 150 mm wafer using a 180 mm diameter target in a tilted PVD target design.

Another attractive advantage of using a tilted target magnetron sputtering system is that it generates a natural thickness "wedge" when the wafer is kept stationary (see Fig. 23). This provides significant benefit for developing thickness sensitive devices, such as the barrier for TMR devices and the copper spacer layer in current-in-plane giant magneto-resistive (CIP-GMR) sensors. The conventional single thickness approach, i.e., fixed layer thickness on each wafer at each time, is not only time consuming, it also introduces uncontrollable wafer to wafer process variations as the device manufacturing takes a few hundred steps from start to finish. Such large number of variables could confound the thickness effect in the final data interpretation. Evidently, if we can make such a thickness change within a single wafer and fabricate multiple devices from this single wafer, wafer to wafer variation will be completely eliminated and it is much more cost-effective as well. Using the "wedge" approach and with pre-determined thickness calibration within a wafer, we can get a layer thickness coverage from 50% of each side of the targetted value, i.e., if the targetted single thickness is x for rotating substrate, we can get a thickness range for a stationary wafer from $0.5x$ to $1.5x$. Thus, we effectively carry out several experiments in one.

There has been extensive development using the wedge approach for CIP-GMR and TMR magnetic device development in the past and these results suit the single

Fig. 22 For tilted target design where $\alpha_1 > \beta_1$ and $d_2 > d_1$. This gives a film with center thin and edge thick at stationary; while for planar design, $\beta_2 > \alpha_2$, which gives a thicker film at center than at edge. However, when the substrate is rotating, the residence time for edge is shorter than center, as a result, more uniform film over larger substrate ($W_1 > W_2$) is achievable for tilted target design on left



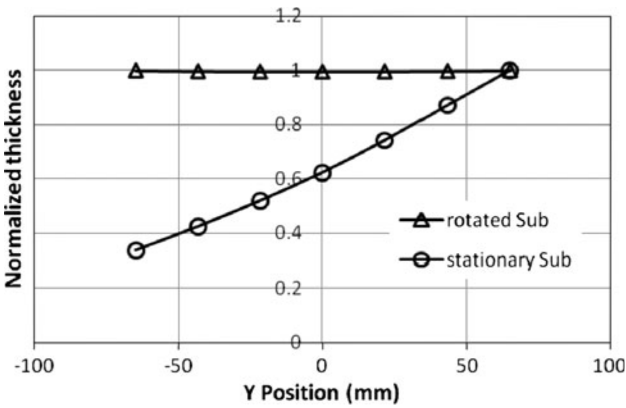
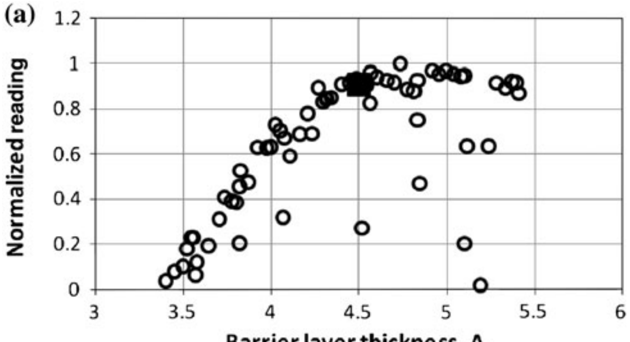


Fig. 23 NiFe film thickness (normalized) across a 150 mm wafer along the wedge direction when substrate was set stationary or rotating for the tilted target sputtering system. It can be seen that the thickness uniformity increased from range over mean (R/M) ~103% (stationary) to 0.5% (rotating) using 180 mm diameter NiFe target and 270 mm target–substrate space and Ar sputtering gas at 0.5 mTorr



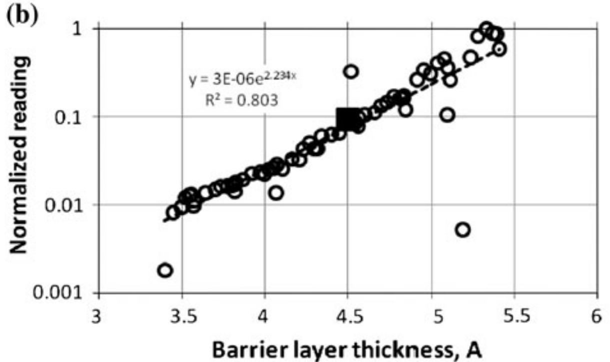


Fig. 24 Normalized TMR ratio (**a**) and the resistance-area (RA) product (**b**) as a function of the barrier thickness. With the barrier layer center point thickness about 4.5 Å, the wedge thickness extends from 3.5 to 5.5 Å range in this case

thickness approach very well, as indicated by the following examples. Figure 24 shows the normalized TMR ratio and RA product for a 0.35 μm diameter TMR device on a 150 mm wafer. The barrier oxide layer thickness with wide range from 3.5 to 5.5 Å on the same wafer has been achieved using the thickness "wedge" approach by setting the wafer stationary on the wafer stage in a tilted magnetron target design. A single thickness point (black solid square) has been included in the plots for comparison and the match between the wedge approach and single thickness is excellent.

Another example to demonstrate the benefit of such a thickness wedge approach is the Cu spacer layer thickness optimization. Copper thickness control is very critical for a bottom spin valve with nano-oxide layer (NOL–BSV) for the stack structure: NiFeCr35Å/CoFe10Å/PtMn120Å/CoFe22Å/Ru9Å/CoFe25Å/Cu-*x*Å/CoFe23Å/NOL/Ta cap [1]. The critical copper spacer layer thickness is usually defined by running a series of single film thicknesses and collecting the GMR ratio, interlayer (between free layer and reference layer via copper spacer) exchange coupling strength, and the sheet resistance of the whole film stack. This conventional one thickness at a time approach is time consuming and has relatively large variation due to the process variables from wafer to wafer as mentioned earlier.

Again the "wedge" approach is more cost-effective and its agreement with the single layer thickness approach is excellent.

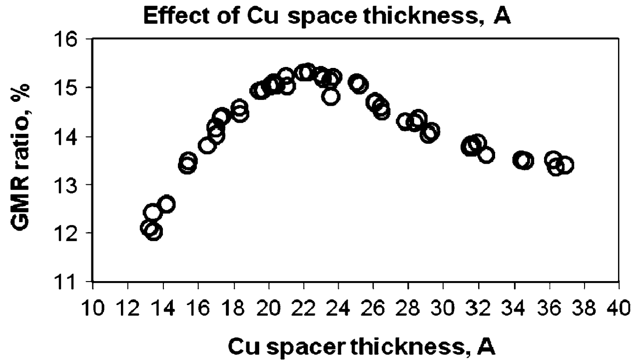
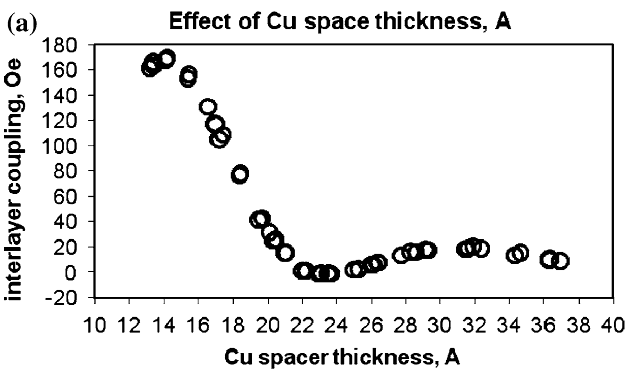


Fig. 25 The GMR ratio as a function of the Cu spacer layer thickness with a peak at the Cu thickness around ~22 Å



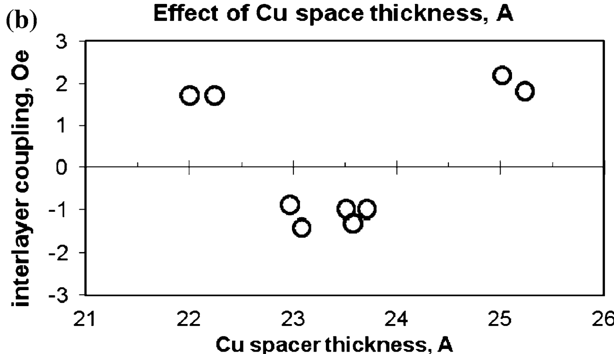


Fig. 26 (a) Interlayer exchange coupling for NOL–BSV with stack: NiCr35/CoFe10/PtMn120/CoFe22/Ru9/CoFe25/Cu-x/CoFe23/Cu6.5/ Al_2O_3-NOL/Ta (thickness in Å). (b) Enlarged portion of (a) from 22.5 to 24.5 Å range to highlight the negative interlayer exchange coupling field

It is evident that the highest GMR ratio is at ~22 Å of Cu (see Fig. 25), matching with the conventional single thickness approach exactly. The interlayer exchange coupling is reduced from positive to negative in the Cu thickness range 22–25 Å (see Fig. 26). As a result, the magnetization of the reference magnetic layer below the Cu spacer and that of magnetic free layer above the Cu spacer will align opposite to each other when Cu is between 22 and 25 Å. This may increase the spin electrons' resistance as the magnetization alignment is in anti-parallel

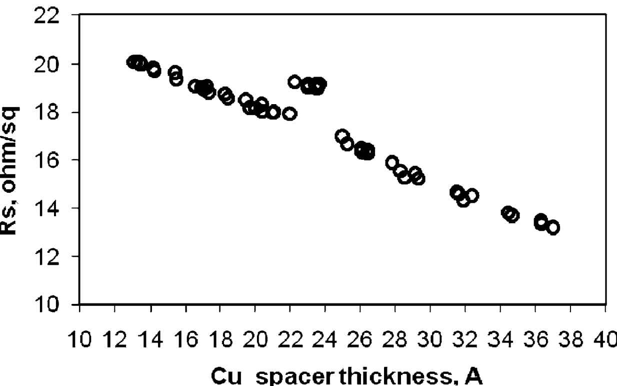


Fig. 27 Sheet resistance R_s as a function of the copper spacer layer thickness. A spike is visible between 22 and 25 Å of copper

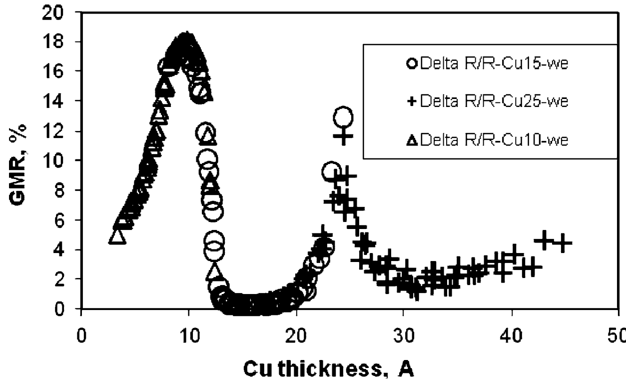


Fig. 28 The two GMR peaks for the trilayer CIP-GMR as a function of Cu spacer layer

direction between the free-layer CoFe and reference CoFe at this region and results in the sheet resistance spike (see Fig. 27). Interestingly, this phenomena is more difficult to observe using an approach with a single Cu thickness each time, due to the potential variation from wafer to wafer.

As a further example, a Cu wedge can be very useful to screen the optimum thickness window in a trilayer CIP-GMR stack: NiCr40Å/CoFe30Å/Cu-xA/CoFe30Å/ NOL/Ta10 CAP is shown in Fig. 28.

The low GMR ratio at around 13–20 Å is due to the fact that the two magnetic layers are ferromagnetically coupled together (magnetization aligns parallel to each other), thus no resistance change in response to the external field would be observed. This has been verified from the magnetization response curve with increased external field strength from −2000 Oe to +2000 Oe.

Target utilization: cusp and shunting magnetron design

Due to the strong electron confinement by the $E \times B$ field or Lorenz force, the electron induced ionization is very much localized on the target surface, which causes

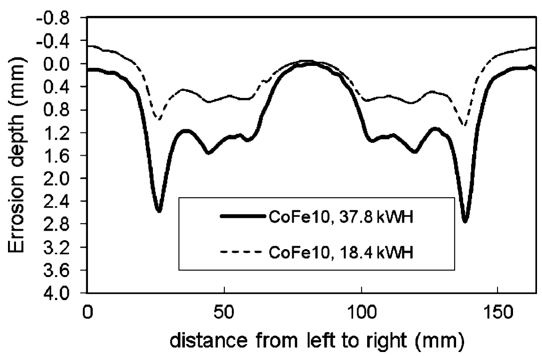


Fig. 29 CoFe target erosion profile as a function of target location (initial target thickness = 4 mm). The localized erosion track development with increased target usage is evident

non-uniform target erosion (see Fig. 29). Such a non-uniform target erosion track gets deeper into the target with extended target usage. At some stage, either the film uniformity will fail the specification or the erosion trench punches through the back plate of the target and causes ejection of back plate atoms into the growing film. So the target lifetime is largely defined by the localized non-uniform erosion rate.

Such non-uniform target erosion introduces cost issues (materials utilization and equipment downtime, productivity loss, etc.). Therefore, it is critical to maintain a high target utilization percentage. There are several ways to improve the non-uniform target erosion profile, by using a CUSP design [31, 32] which spreads out the erosion profile into many smaller regions, or by using a magnetic shunting design [33]; therefore, it prevents the erosion trench getting deeper by shunting the magnetic field in these fast eroding locations from the back of the target, resulting in reduced electron trapping there and reduced ion impingement.

An example on how to optimize the thin film properties via process parameter tuning for a fixed hardware setup

For any targeted thin film application, once the hardware design is completed and fixed, tailoring the process window is required to meet the specific application requirements. Here is presented an example of a thin copper layer for a GMR device. A thin (a few tens angstroms) copper layer is usually required for such a device (dimension: $\sim$50 nm (width) $\times$ 50 nm (length) $\times$ 30 nm (height)). Film thickness uniformity and resistivity uniformity across the substrate are two important parameters for device performance control.

There are three parameters which can be tuned for such copper film property control, namely, gas flow, sputter power, and target–wafer separation distance. Usually, higher power and lower gas flow provide better film thickness and resistance uniformity. However, higher power has the tendency to generate high energy neutrals and promotes more interface mixing, which is undesirable for such thin film devices. Lower power ($<$50 W, for instance) sputtering, on the other hand, provides much less inter-mixing between thin film layers, but it suffers from plasma instability. Higher pressure (usually achieved by raising the Ar flow rate) increases the gas phase collision probability and thus reduces the energy of neutrals and ions, but it favors small grains and less-dense film formation. Therefore, carefully balancing film uniformity and microstructure is important for an optimized process. The target–wafer separation has less impact on the film uniformity in the tilted target design, but increased target–wafer separation can reduce energy of impinging atoms/ions on the growing film at the price of reduced film growth rate, due to the high probability of gas phase scattering of ejected atoms from the target surface (see Fig. 30).

Impedance change during RF sputtering of dielectric materials

Magnetron sputtering has been used not only for metallic film deposition but also for dielectric layers, though an RF or pulsed bipolar sputtering power source needs to be used for insulating dielectric films. One of the process control challenges is that film deposition rate drifts with extended process time during such dielectric film formation (either by direct RF sputtering from a dielectric target or by reactive sputtering from metallic target). It is apparent from Fig. 31 that it takes about six wafers to stabilize the MgO film thickness (deposition rate), due to the increased insulating MgO coverage on the shielding, which changes the system capacitance. The precise MgO barrier layer thickness control is vital for the TMR device performance (such as resistance $\times$ area (RA) product and TMR ratio). Choi et al. [3] reported that sputtering a thin metallic layer between wafer runs is effective to control such MgO thickness/deposition rate drifting. The exact mechanism is still unknown though; it is suspected that the dielectric layer (MgO, TaO, Al_2O_3, etc.) deposition onto the metallic chamber wall and shielding surface alters the system impedance and the RF matching. As a result, the plasma potential and the wafer stage self-biasing (floating potential) will drift, which in turn affects the film thickness and properties.

Such metallic layer “pasting” is also effective to control dielectric layer thickness drift in reactive sputtering of a TaO insulator layer as shown Fig. 32. In a conventional process, the film thickness (or deposition rate) drops off with increasing processed wafer numbers and tends to stabilize after about 10 wafers. Adding a 50 s deposition of a metal layer, such as Ta, Al, Mg, Ti, etc. (the stage is covered by a shutter and the rest of chamber will subject to

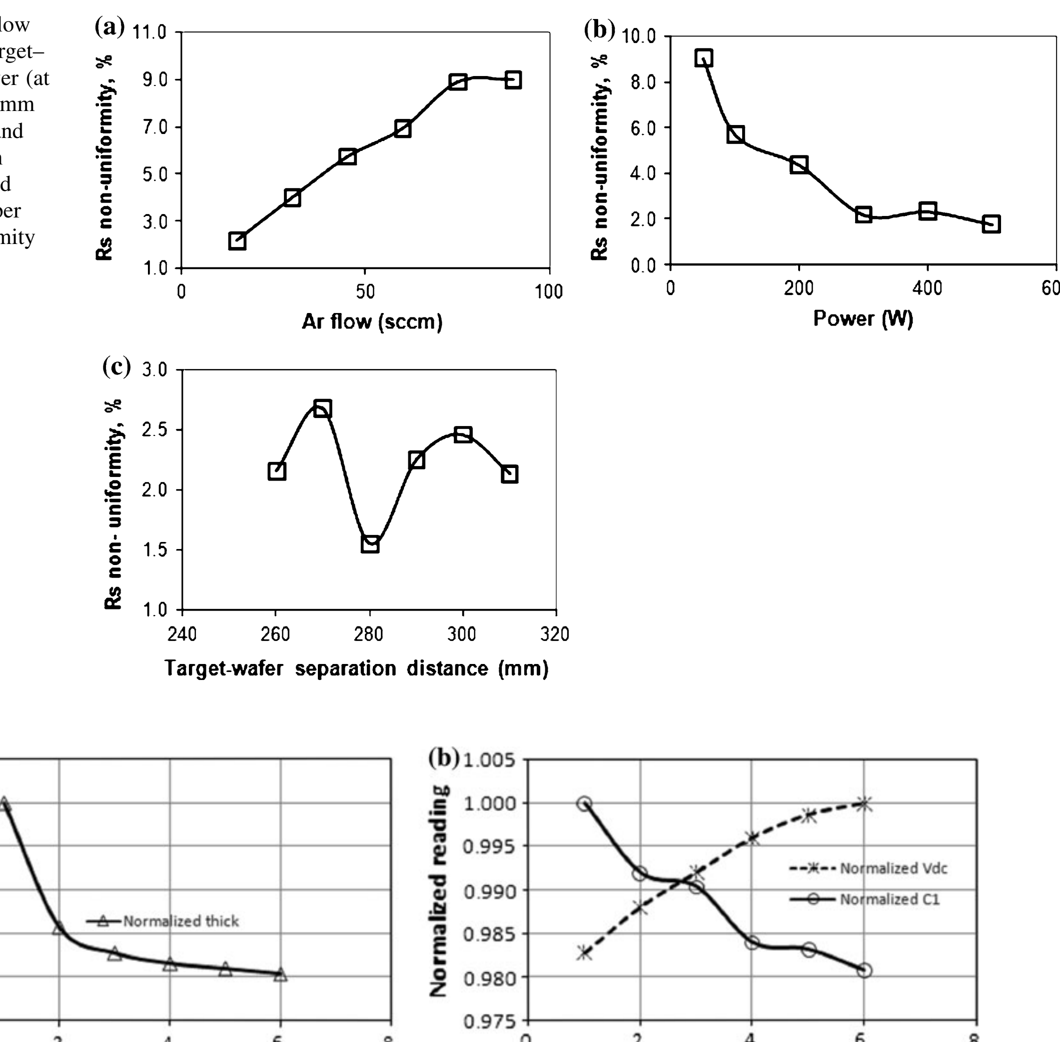


Fig. 30 Effect of (**a**) Ar flow (at 300 W and 260 mm target–wafer separation), (**b**) power (at 15 sccm Ar flow and 260 mm target–wafer separation), and (**c**) target–wafer separation distance (300 W power and 15 sccm Ar flow) for copper thin film resistivity uniformity across 150 mm wafer

Fig. 31 Normalized (**a**) MgO thickness and (**b**) DC self-biasing voltage (V_{dc}) and matching box capacitor position (C_1) as a function of wafer ID prepared via RF sputtering from MgO target

the metallic layer "flashing" during this metallic layer deposition) between each TaO wafer process, the deposition rate drift slows down significantly (Fig. 32). The metallic layer during such a "flashing" step is presumed to restore the metallic behavior of insulating TaO covered shielding and chamber wall. From Fig. 32 the wafer to wafer thickness variation is much improved with 50 s of metallic layer flashing, though it still drops down. It can be expected that the TaO deposition rate will flatten out with increased metallic "flashing" time to over 50 s. However, this is at the price of reduced throughput.

Substrate temperature control during magnetron sputtering

The substrate temperature during ultra thin film deposition significantly influences its microstructure development and film morphology. For example, in a TMR device, the thickness of some critical layers (tunneling barrier layer and Ru anti-ferromagnetic coupling layer) is only a few angstroms. The film growth conditions, such as substrate temperature and energetic species impingement, significantly alter the properties and growth mode of such layers. Fujikata et al. [34] reported that the roughness of an Al barrier layer can be dramatically reduced by lowering its deposition temperature to below −50 °C (Fig. 33).

As a result, Shimazawa and Tsuchiya [35] reported that the resistance change from wafer to wafer for a TMR device with Al_2O_3 tunneling barrier can be substantially reduced when such a Al_2O_3 barrier is formed by deposition of Al at liquid nitrogen (LN_2) temperature and followed by oxidization; while the TMR ratio is nearly identical (see Fig. 34). The LN_2 temperature deposition gives much

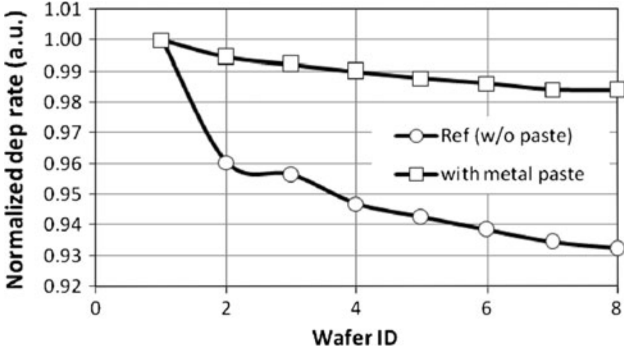


Fig. 32 Normalized deposition rate of reactive sputtered TaO film as a function of wafer number. Those without metal paste in-between wafers and those with ~50 s of metal paste in-between wafers are plotted here for comparison. (DC power = 1.2 kW, pressure = 5 mTorr, Ar/O_2 flow = 50/25 sccm)

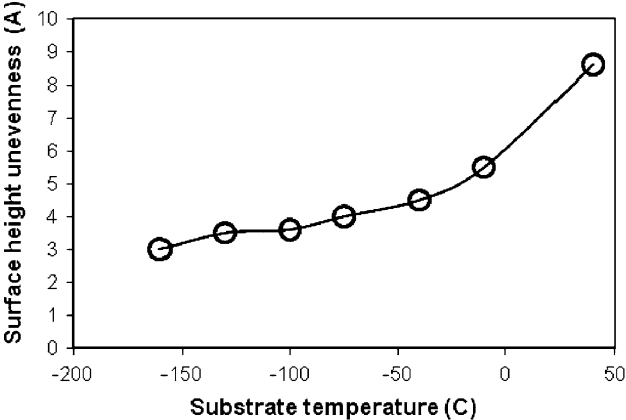


Fig. 33 Aluminum layer surface unevenness in angstrom as a function of its deposition temperature for a typical TMR stack: NiFe/Co/Al–AlO_x/Co/NiFe/FeMn/NiFe/(substrate)—re-plot from Fujikata et al. [34]

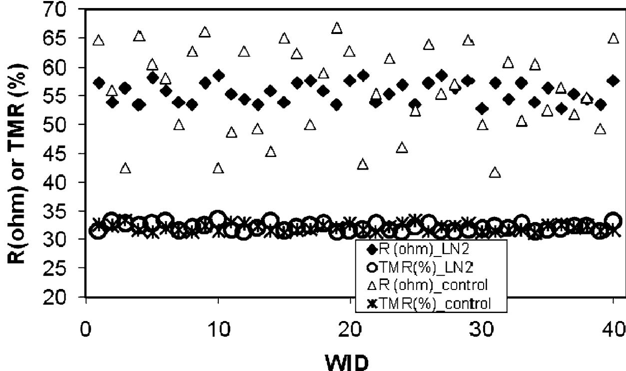
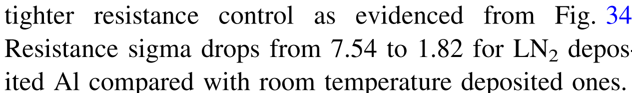


Fig. 34 0.6 × 0.6 µm device TMR ratio or resistance variation from wafer to wafer for room temperature deposited Al and LN_2 temperature deposited Al barrier in a TMR stack (layer thickness in Å): Ta30/NiFe50/CoFe5/Al7-ox/CoFe30/Ru7/CoFe20/PtMn150/Ta30—re-plotted from Shimazawa and Tsuchiya [35]



tighter resistance control as evidenced from Fig. 34. Resistance sigma drops from 7.54 to 1.82 for LN_2 deposited Al compared with room temperature deposited ones.

This is largely due to the formation of much smoother Al layer at lower temperature where Al grain growth via diffusion is almost "frozen". Similar temperature effects have been found on the microstructure development of other magnetic layers as well. For instance, a CoFe$_x$ layer is usually in a crystalline state, while it changes to amorphous at a lower temperature of <-50 °C. This is critical for the MgO TMR device, as the MgO (001) texture only develops on an amorphous layer [36] (such as CoFeB amorphous magnetic layer) or a crystal substrate with lattice well-matched with MgO, such as iron [37].

However, lower temperature deposition reduces throughput. From Shimazawa's report [35], cooling from RT to 150 K requires 30 min; while warming it up to RT takes another 45 min. With a faster cooling/heating stage design, such time can be reduced. It is a trade-off between performance, process controllability, and cost eventually.

Particle prevention

During sputtering, the ejected atoms from the target not only land onto the wafer surface, but also impinge on the shielding and chamber wall and build-up there. As such building up gets thicker and thicker and once the stored strain energy exceeds the interface bonding strength (or adhesion) between the building up and its substrate, it starts to peel off and may fall onto the growing film surface and cause defects. Figure 35 shows such material peeling off from the cathode shielding after 23 kWh of target usage.

There are several ways to minimize the particle risks, such as grit blasting the shielding to increase its surface roughness (hence improving build-up layer adhesion), changing the shielding after a certain amount of target lifetime (at the cost of increased equipment downtime).

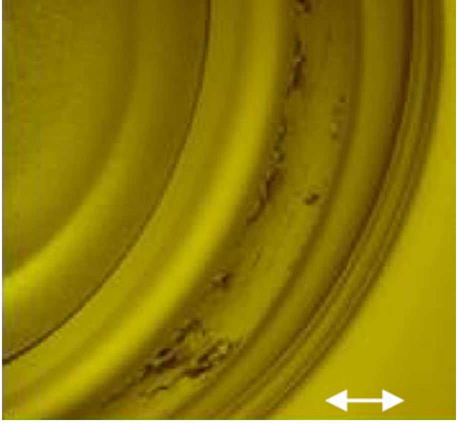


Fig. 35 Severe flaking from the cathode shielding after 23 kWh sputtering for one of the target material. *Arrow* = 20 mm

The tilted target design actually also helps to minimize the particle risk as the wafer stage is off-centered relative to the target center and particles have less probability to fall onto the wafer surface, compared with the planar target configuration. Minimizing the arcing also suppresses the particle generation.

Arcing

When the discharge current reaches a certain level, the impingement of the cathode surface by the ion flux generates substantial local heating to a point where thermionic electron emission occurs. These thermionic electrons cause the cathode sheath to collapse and arcing (i.e., very localized sparking) appears on part of the cathode surface or across the cathode/cathode shield gap. At such arcing locations, the massive energy densities could cause material melting, particulate ejection, and wafer damage. For high rate DC and RF sputtering systems, arcing is thus a potential concern and needs to be prevented.

For insulating material deposition by reactive sputtering, localized insulating spots on the cathode surface could result in a high electrical field build-up and thus cause arcing. This could be a particular problem for ultra thin film wafer processing as it causes thickness non-uniformity and damage to the growing layers. Arcing could also be related to the local high gas pressure spikes on the target surface or the flaked particles within the gap between cathode (active) and cathode shield (grounded), which will partially short the gap under high electric field. Though out-gassing from target voids/cracks and insulating particle inclusion (see Fig. 36) could also be the arcing sources, their occurrence probability though is relatively low for modern ultra high purity sputtering targets, particularly those for ultra thin film processes requiring thickness control accuracy in the angstrom range and purity levels >99.99%.

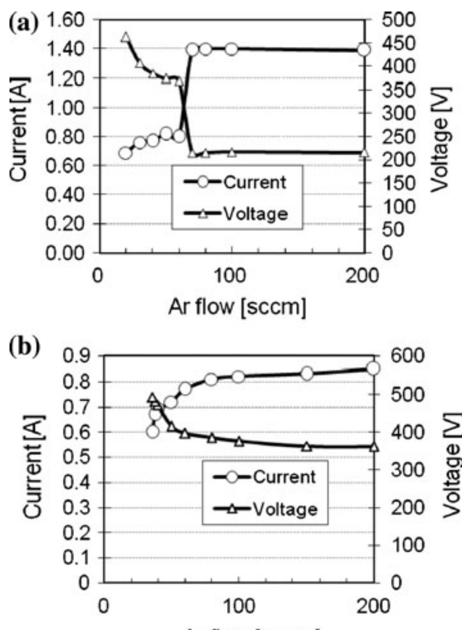


Fig. 37 (**a**) Arcing and (**b**) “normal” discharge I–V curves for Cu sputtering at 300 W, 0.5 mTorr pressure, and target/substrate separation of 260 mm

Fortunately, such arcing can be easy detected from the discharge I–V curves as shown in Fig. 37. Such local arcing causes the discharge voltage to drop and the current to increase. A sharp I–V curve is noticeable in Fig. 37a, compared with the smooth I–V curve in Fig. 37b for a normal discharge.

Besides the sputtering process parameter window optimization and target quality control, power supply design plays a substantial role in avoiding arcing-related damage by minimizing the stored energy in the power supply’s output, thereby reducing arc energy, and by a rapid detection of the arc and quick shut-off the power supply.

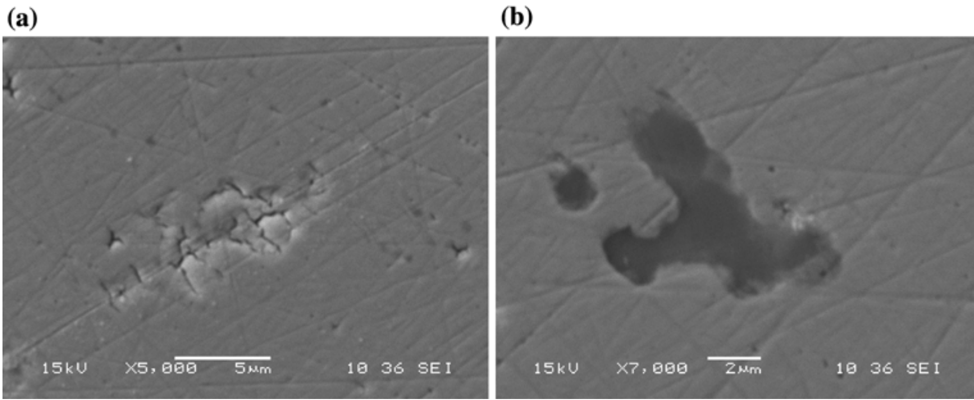


Fig. 36 (**a**) Cracks/voids and (**b**) MnO_x–SiO_x inclusion within an IrMn target during the incorrect target processing. Arcing could be triggered if there is a trapped gas from such cracks/void or around the insulating MnO_x–SiO_x locations during the DC sputtering

Target cracking/contamination

The strong ion bombardment during the magnetron sputtering process can transfer substantial energy to the target and heat it up to high temperature. If the target is not properly bonded to the back plate or the water cooling is not sufficient (particularly for high power sputtering), the target could crack, deform, debond locally or even detach from the cathode. The picture in Fig. 38a shows the front side of a cracked target and the melted bonding materials infiltrated to the top surface via such cracks.

Surface contamination (caused by the re-deposition of target atoms onto the center of the target, where the magnetic field is weak and electron density is low) as shown in Fig. 38b should also be avoided. Such re-deposited material could be a few millimeter thick in some cases. Such material re-deposition onto the center of target can be reduced by redesigning the non-symmetrical magnetron and making sure the erosion tracks are moving across the whole target and avoiding the "dead-zone"—where material is re-deposit.

Ion Beam Deposition (IBD)

Typical set up

IBD differs from magnetron sputtering in several aspects. The atom flux for film growth is generated from a target surface by the energetic impingement of a separate ion beam (broad beam or focused ion beam) created far away from target surface. The target erosion is limited to a small section if a focused beam is used, which results in lower target utilization. It does provide better contamination control as the ejected atoms are primarily coming from the target center and minimize contamination from the target edge and its surrounding shielding. A broad beam ion source, on the other hand, provides more uniform target erosion and thus high target utilization ($>\sim 50\%$), but the materials from the target edges and surrounding shielding may also be sputtered out and incorporated into the growing films.

In IBD systems, the angular distribution of the ejected atoms and their dependence on the incident beam energy and angle [38, 39] can be manipulated depending on application. Further, the ion beam is usually neutralized after exiting the beam grids, so it can be used for both dielectric and metallic film deposition without arcing concerns.

The substrate is usually facing the target with the growing film side placed downwards (for particle prevention) and off-centered by some distance (d, as shown in Fig. 39). The off-center distance between the wafer and target, together with the wafer angle (relative to the target) are critical parameters for the film uniformity control. This, to some extent, is similar to the tilted magnetron design discussed above. As the wafer angle (α) or the target angle (β) changes, the acceptance angle of the ejected atom flux from the target received at the wafer center and edge varies. This causes film uniformity changes. As the wafer is usually rotating during film deposition, a configuration enabling faster edge deposition than at the center will favor more uniform film thickness.

Angle dependent film deposition rate and uniformity

Figure 40 shows the normalized Ta sheet resistance (R_s—inversely proportional to the thickness) as a function of the wafer angle (α). Note that the film R_s pattern changes from center high to edge high with increased angle from below 40° to above 60°. As shown in Fig. 41, within wafer film uniformity peaks (range over mean <3% for 200 mm wafer) at about 40° wafer angle with relatively high deposition rate. A 90° wafer angle also gives good uniformity, but it suffers lower deposition rate due to the ejected atom

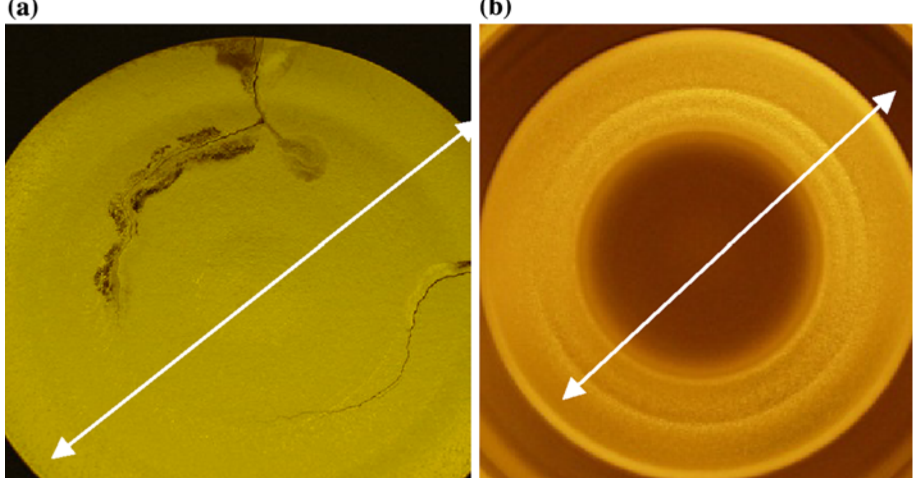


Fig. 38 (**a**) Through target cracking (imaged is the front side of the target-bonded to the water cooled Cu back plate. *Arrow* = 180 mm. (**b**) Center re-deposition caused contamination of the target due to there is less ion bombardment. *Arrow* = 300 mm

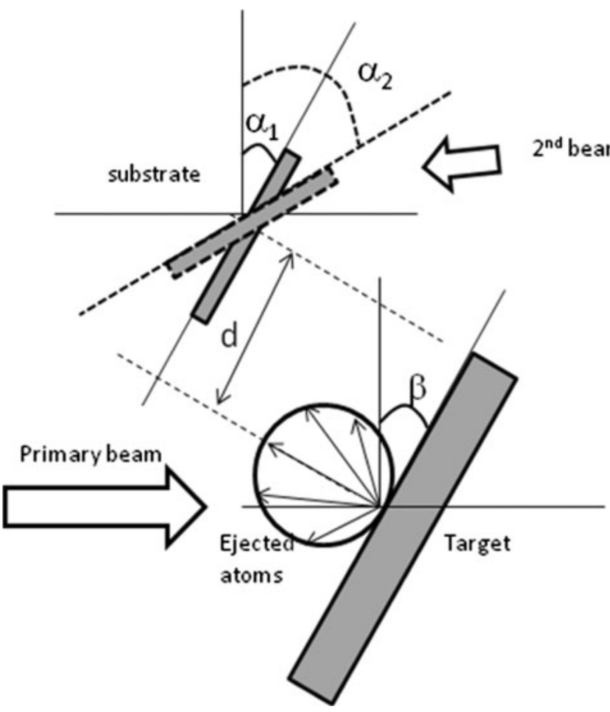


Fig. 39 Schematic drawing of the target and substrate configuration in a typical ion beam deposition system used in this study

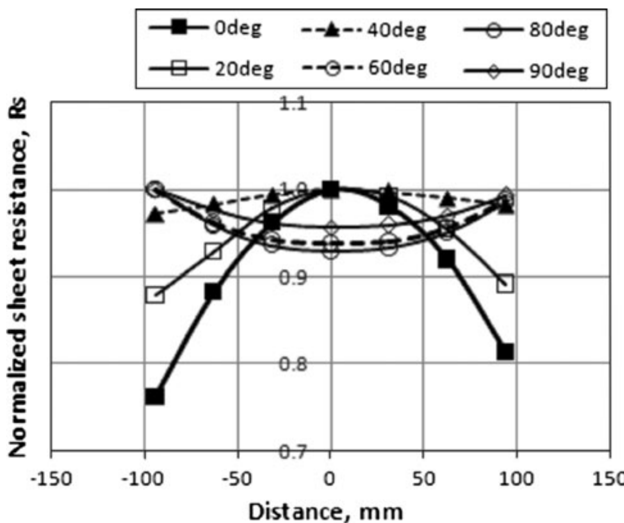


Fig. 40 Normalized Ta sheet resistance uniformity across the wafer along the notch direction as a function of wafer stage angle (α) during IBD deposition (beam voltage = 1500 V, current = 200 mA, RF power = 400 W. Target angle, $\beta = 40°$). Wafer size = 200 mm

trajectory distribution as shown in Fig. 39. Other materials ($CoFe_{10}$, for example) have shown a similar deposition rate trend with varied wafer angle to Ta (see Fig. 42).

It should be pointed out here that such an angle dependent deposition rate is universal, though the actual wafer angle may be different depending on the hardware configuration. Figures 43 and 44 illustrate the deposition

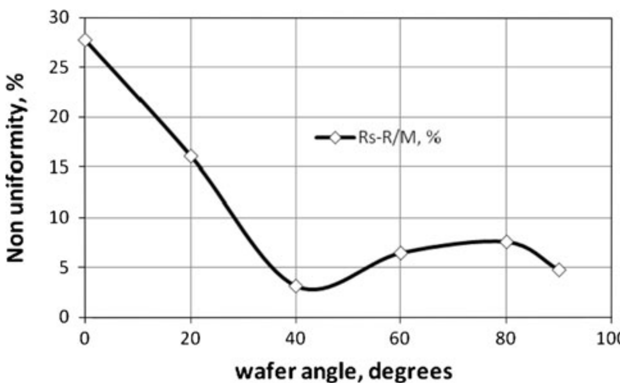


Fig. 41 The R_s non-uniformity (range over mean) as a function of the wafer angle for Ta (beam voltage = 1500 V, current = 200 mA, RF power = 400 W. Target angle, $\beta = 40°$). Wafer size = 200 mm

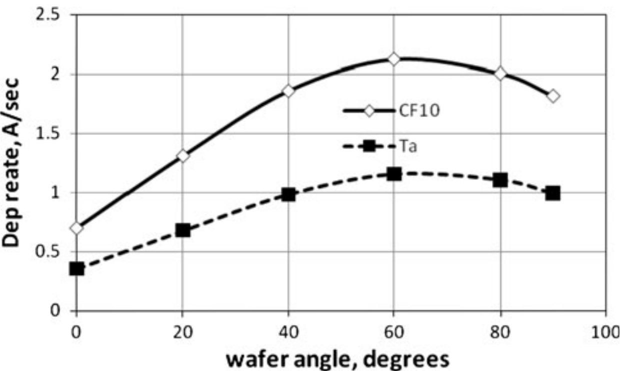


Fig. 42 Deposition rate as a function of wafer angle for $CoFe_{10}$ and Ta. It shows a maximum deposition rate at about ~60° for this system-B (beam voltage = 1500 V, current = 200 mA, RF power = 400 W. Target angle, $\beta = 40°$)

rates for (CoPt), (TiW), and (Al_2O_3), respectively, in another type of IBD system. The peak deposition rate in this system is at about ~130° (with 360° tilt capability) for all the above three films. The ion beam conditions are: beam voltage = 300 V, beam current = 220 mA, RF power = 150 W. Either Ar or Xe has been used as the working gas for the ion beam.

Angle dependent texture development

We pointed out early that in an IBD system, the plasma source is placed far away from the growing film surface. This could be potentially useful to minimize the film damage caused by the energetic species impingement and UV radiation from the beam source. However, for some film growth, some degree of energetic bombardment is required to favor a specific crystalline texture growth.

For a CoPt hard bias magnet commonly used for a magnetic reader sensor, for instance, it is important to maintain a high coercivity (H_c) for this material, which

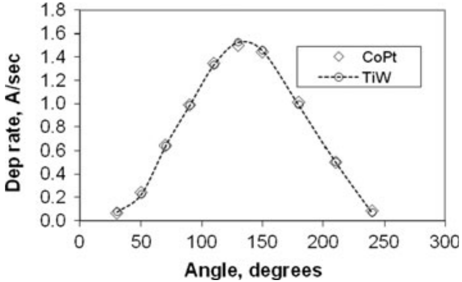


Fig. 43 IBD CoPt and TiW deposition rates as a function of wafer stage angle. A maximum deposition rate is found to be around 130° stage angle in this system

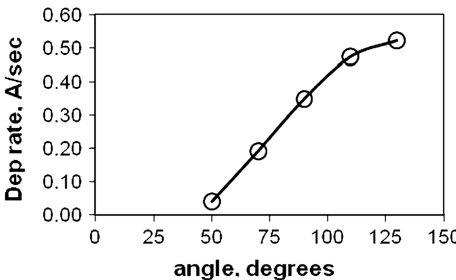


Fig. 44 Al_2O_3 sputtering rate as a function of wafer stage angle (only one side of the data are shown here, it is symmetrical relative to the stage angle above 130°–210°). It shows a max deposition rate at ~130° stage angle in this system

requires correct film texture. Due to the angular distribution of ejected CoPt atoms from IBD target surface, the incident CoPt atom flux angle relative to the wafer surface can be altered from perpendicular to the wafer surface to the glancing angle by tilting the wafer stage. To facilitate high coercivity CoPt growth, a glancing angle incoming growth atom flux is preferred, though this results in reduced deposition rates. This is why when the CoPt atom flux arrives perpendicularly at the growing film surface (130°, for example), the H_c is low; while at glancing angle (210°, for example) or after adding a secondary ion beam bombardment at an angle of ~40° from film surface normal, the H_c increases (see Fig. 45). This ion bombardment is believed to favor a CoPt C-axis orientation change from out-of-plane to in-plane. As a result, the normalized coercivity of the CoPt increases when impinging CoPt flux atoms are at glancing angle or with the assistance of a second ion beam bombardment surface during the film growth.

Step coverage control

Increase step coverage Step coverage is important in thin film nano-device fabrication. For instance, high step coverage is beneficial for electrical isolation and uniform seed layer deposition. However, in other cases, such as the CoPt

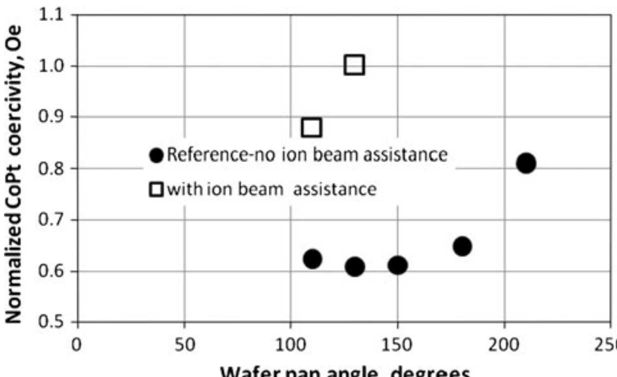


Fig. 45 Normalized CoPt film coercivity (H_c) for 200 Å thickness grown on Ta/TiW seed layer as a function of wafer pan angle. (*Note*: ~130° is the position where wafer and target surfaces parallel to each other. Assistance ion beam condition: 300 eV, 40 mA Ar^+ or Xe^+)

hard bias magnet deposition, less CoPt step coverage is required to avoid the CoPt flux being shunted to the top NiFe shield layer.

As pointed out earlier, the wafer position relative to the ejected atom flux direction can be easily manipulated in an IBD system. This feature is useful when IBD is used to deposit films across a junction with conformal coverage. Although it is still inferior compared to atomic layer deposition (ALD) in terms of conformality of coverage, it is much better than conventional sputtering, particularly for devices well-separated from each other, like magnetic recording sensors.

Figure 46 shows schematically how such a relative angle can affect the step coverage. In Fig. 46a the incident atom flux is tilted to an angle relative to the junction normal. As such, the film growth on the junction sidewall will be relatively thin. Note that both the incident atom flux and the resputtered atom from the field area contribute to the film growth on the side wall in Fig. 46b. With the increase of the relative angle between the wafer normal and the incident atom flux, side wall film growth can be made comparable to that on field area (see Fig. 46c).

This is further demonstrated in Fig. 47a–c. The step coverage (the ratio of side wall film thickness over bottom field film thickness) for an IBD deposited Al_2O_3 isolation layer can be changed from 300 to 50% when the wafer stage angle relative to the beam is altered from 50° to 90°.

Minimize step coverage For some other nano-device fabrications, we will need to minimize the step coverage. As described above, the step coverage depends on the actual atom flux incident angle relative to the normal of the local device surface to be covered. Therefore, the device profile has a strong impact on its step coverage.

For a nearly vertical device junction and vertical deposition atom flux as shown in Fig. 48, side wall film growth

Fig. 46 Schematic drawings showing (**a**) relative angle between the junction normal and incident atom flux, (**b**) the side wall film growth, and (**c**) >100% step coverage (side wall thickness over field region thickness) at 80° incident atom flux for CoPt film around a junction

Fig. 47 IBD Al_2O_3 (white material) step coverage from (**a**) 300%, (**b**) 130% to (**c**) 50% by varying the wafer angles from 50°, 70° to 90° for a typical junction

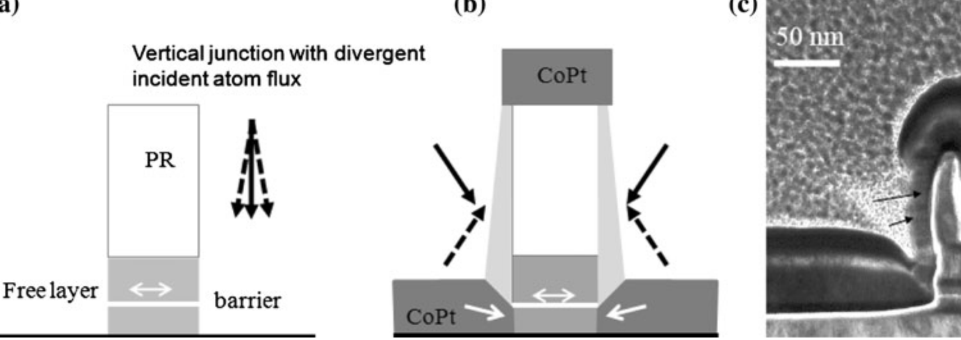


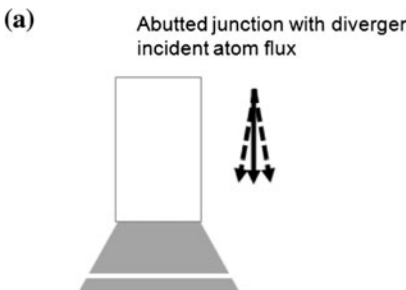
Fig. 48 Schematic drawing showing (**a**) the vertical junction and a vertical incident atom flux with a divergence angle. (**b**) The resulted less-dense sidewall film growth and (**c**) a TEM cross-section image showing the columnar CoPt film structure on side wall. *Arrows* in (**c**) indicating the incoming atom flux direction during the sidewall CoPt growth

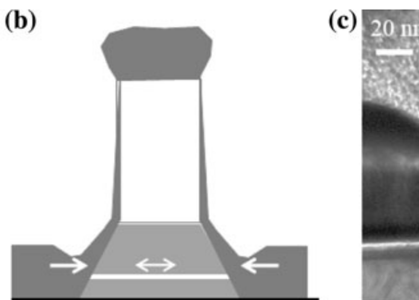
and its microstructure resulted from either the angular distribution of incident atom flux or the self-sputtering of growing film in the field area and re-deposition onto the side wall can be very different from those in field area (see Fig. 48a, b). For example, when the incident CoPt atom flux is perpendicular to the bottom surface in a TMR device fabrication, the lateral sidewall CoPt growth is detrimental. Since the microstructure and magnetic properties of CoPt grown on side wall are different from that grown in the field area. Such less-dense CoPt layer formation along the sidewall of a TMR device junction increases the separation between the more dense CoPt film and the edge of the magnetic free layer (above the white line-barrier layer in Fig. 48c). This causes the under biasing the free layer of the magnetic device as the magnetization (indicated by the white arrow shown in the sketch) from CoPt points downwards and away from free layer.

The above issue can be partially solved by increasing the junction slope angle (see Fig. 49) or by tilting the target/wafer relative angle to enable sufficient incoming flux to reach the corner of the junction. However, this will create significant side wall coverage of the CoPt layer on the junction wall and results in magnetic flux shunting to the top shield. An extra process step can be added to remove/minimize such magnetic flux shunting to the top NiFe shield layer though at the penalty of increased process complexity.

PECVD

For some thin film nano-device processes, both low temperature deposition (minimizing the thermal load) and conformality (maximizing the film uniformity and step coverage across large topographic features) are required. Certainly, IBD film deposition can be done at near room temperature and its step coverage is tunable to some extent. The thermal CVD process is known being capable of good conformality, but may require higher deposition temperature beyond the tolerable range for some applications. ALD has been proven to be an attractive conformal thin film





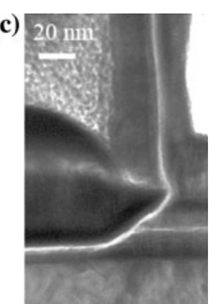


Fig. 49 Schematic drawing showing (**a**) a sloped junction profile, (**b**) the side wall coverage at vertical incident atom flux, and (**c**) TEM cross-section of CoPt hard bias magnet profile deposited on a slopped TMR device

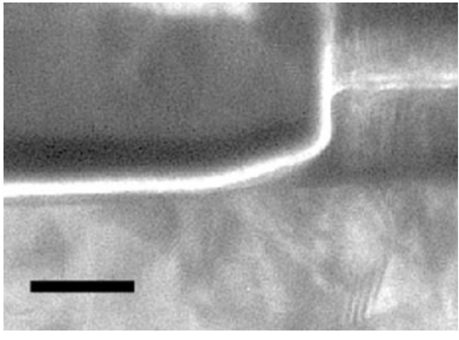


Fig. 50 Conformal coverage of a ~3 nm SiN deposited by PECVD at 150 °C across a nearly vertical magnetic device. (*Scale bar* = 20 nm)

technology at low temperature (<~300 °C). However, suitable ALD precursors could be very limited and expensive. PECVD has been widely used to meet the need for lower temperature and has reasonably good conformality for nano-scale device fabrication. As shown in Fig. 50, 30 Å of UHF PECVD SiN deposited at ~150 °C wafer temperature provided excellent step coverage for a vertical TMR tunneling device and its electric isolation performance is comparable to ALD Al_2O_3, but at much lower cost.

Reactive species concentration effect

To initiate a film growth on any substrate, reactants need to be transported to the substrate surface and initiate the surface reaction there. Therefore, the film growth (deposition) rate will be determined by the minimum of the above two competing reactions: mass transportation from the gas phase to the substrate surface (R_m) and the kinetics of the surface reactions (R_s), i.e.

$$R \Rightarrow \text{Minimum}\{R_s, R_m\} \tag{14}$$

For a compound film growth, such mass transportation is further limited by the minimum concentration of all involved reactant components. For SiN formation, this includes both the [Si–] and [N–] containing species concentrations.

$$R_m \Rightarrow \text{Minimum}\{[C_{(Si)}], [C_{(N)}]\} \tag{15}$$

The surface reaction is largely driven by the activation energy (E_a) and substrate temperature (T) at a fixed diffusion coefficient (D_0):

$$R_s \propto D_0 \exp\left(\frac{-E_a}{kT}\right) \tag{16}$$

If $R_m \ll R_s$, the film growth rate will be limited by the R_m (growth governed by the mass transport).

If $R_s \ll R_m$, the film growth will be controlled by the R_s (surface reaction dominated growth).

SiO_xN_y has been used for the bottom anti-reflective coating (BARC) for photo patterning and as a carbon etching hard mask [29] in magnetic sensor fabrication, which requires deposition temperatures <250 °C, to minimize the inter-diffusion between ultra thin (~a few angstroms to a few tens of angstroms) magnetic layers. The PECVD system used in this study is manufactured by Unaxis. The 13.56 MHz RF power was coupled via the top electrode. Both wafer stage and the chamber were grounded. Reaction gases were introduced from the showerhead via the top electrode. The gap between the showerhead and wafer stage is about 3 cm. The wafer stage temperature is controlled via a heat exchanger from 130 to 300 °C. The overall chemical reactions of SiO_xN_y can be expressed as below.

$$SiH_4 + N_2O + NH_3 \Rightarrow SiO_xN_y + H_2 + N_2 \tag{17}$$

It is clear from the above Eq. 17 that the deposition rates depend on the supply of all the reactants.

Figure 51 shows that SiO_xN_y growth rate increases with the increase of RF power as more active Si-containing species are dissociated at higher power level. Assuming 25 sccm of SiH_4 is fully dissociated above 100 W RF power and the diffusion boundary layer is thin enough, SiO_xN_y growth is limited by the lack of a Si-containing precursor supply from the gas phase when O and N are over-saturated. Thus the growth rate flattens out above 100 W RF power. Increasing the SiH_4 flow from 25 to 75 sccm pushes the growth rate saturation knee to a power level of above 300 W.

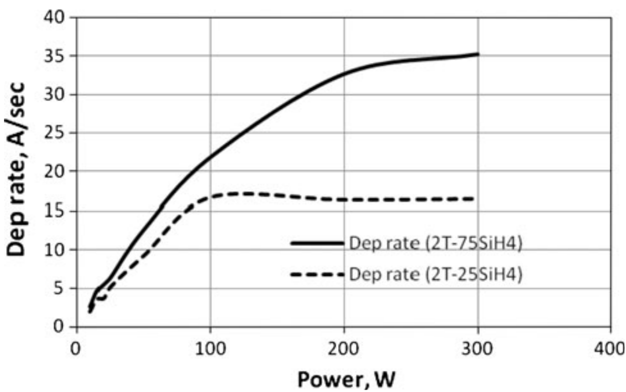


Fig. 51 PECVD SiO_xN_y deposition rate at 2 Torr and 250 °C, 10 sccm N_2O flow, 50 sccm He, and 25 sccm NH_3, diluted by N_2 (2000 sccm total flow). Two SiH_4 flow rates: 75 sccm (*solid line*) and 25 sccm (*dashed line*) were plotted here

Similar mass transportation limited growth has also been observed during SiN deposition processes in a different tool configuration excited by a 60 MHz UHF RF source. The SiN formation reaction can be expressed as follows:

$$SiH_4 + NH_3 \Rightarrow SiN + H_2 \quad (18)$$

Again, the SiN growth rate will depend on the supply of SiH_4 and NH_3 species. For the 150 °C deposition case shown in Fig. 52, at less than 20 sccm of (10% SiH_4–Ar) flow rate, SiN growth is limited by the supply of Si-containing species, while above 20 sccm of (10% SiH_4–Ar) flow rate, the SiN film growth is governed by the NH_3 supply. i.e., on the left hand side of the dashed line it is limited by Si-species concentration, while on the right hand side of the dashed line it is limited by the NH_3 species supply. Increasing the NH_3 supply will further increase the SiN deposition rate until the Si-containing species concentration becomes the limiting factor again (see the sketch in Fig. 53).

Similarly, SiO_xN_y growth rate will depend on the mass transportation from O, N, and Si. As the plot in Fig. 54 shows that above ~14 N_2O/SiH_4 ratio, the SiO_xN_y growth rate starts to saturate. However, part of the complexity here is that the O and N will compete for the available Si source and the stoichiometry of the film will be changing.

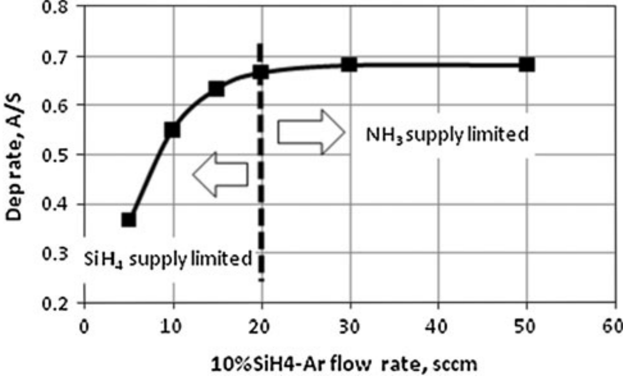


Fig. 52 High density plasma CVD SiN deposition rate as a function of Ar diluted 10% SiH_4 flow rate at a fixed RF power of 700 W (pressure = 120 mTorr, NH_3 flow = 50 sccm, stage temperature = 150 °C)

It is apparent that with ever-increasing N_2O flow, the deposition rate tends to be flattened out due to the consumption of SiH_4 by N_2O and forms SiO_xN_y. This reaction will eventually be self-limited after the dissociated SiH_4 species are fully consumed by excess N_2O and further increase in N_2O will not lead any deposition rate increase.

Film thickness uniformity improvement examples

Understanding the above film growth limit steps is critical for hardware modification and corrections during process development. Figure 55 shows the impact of NH_3 gas inlet port design in an UHF CVD setup on the non-uniformity of SiN film. When single NH_3 gas inlet port is used, SiN non-uniformity is at ~5% (range/mean), while a symmetrically located double NH_3 gas inlet port reduces this non-uniformity to ~2%. This is because in the UHF CVD process in the above setup, NH_3 is first cracked by RF, then the reactive NH_x species (x = 0–3) react with SiH_4, injected from the outside the discharge zone (to minimize Si gas phase nucleation). From the previous discussion we know that the SiN deposition rate depends on the available concentration of both [N] and [Si]. Due to the small flow rate (~50 sccm) of NH_3, the [N] content away from the NH_3 injection port drops quickly if the pressure is not high enough and the film growth slows down away from the NH_3 injection port due to reduction of available reactant. High film non-uniformity results. By using the double NH_3 injection ports, the NH_3 distribution within the whole shower head is much more uniform and the resulting SiN deposition rate becomes more uniform across the whole wafer. Film non-uniformity (range/mean) improved to ~2% (see Fig. 55b).

Plasma-based thin film removal techniques

After thin film stack deposition, further patterning is required in order to define functional units and link them together. Such a patterning process involves photo lithography, pattern transferring via material removal, and the electric insulation/connection and final package. Material removal can be achieved by several methods, such as a focused energetic process (laser ablation), mechanical force (scribing), chemical reaction from solvent (wet etching), and chemical or physical removal by radical/ion bombardment (plasma-based etching), which we shall focus on in the following sections.

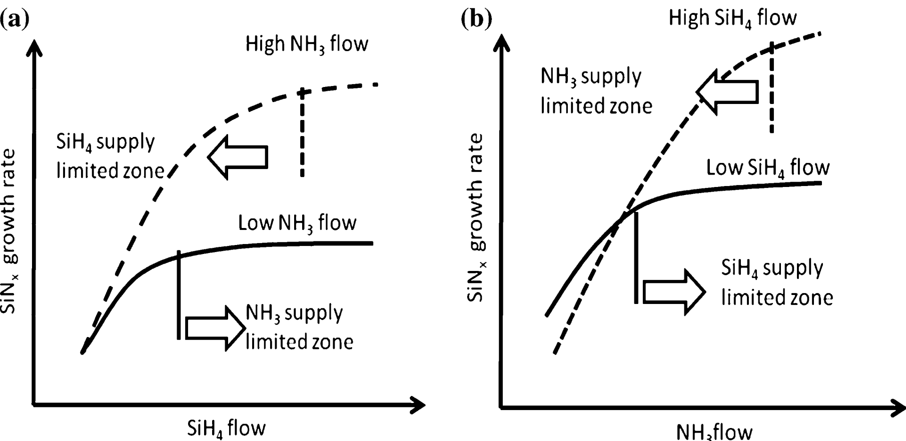


Fig. 53 Schematic drawing showing the mass supply limited SiN growth model as a function of (**a**) SiH_4 flow rate and (**b**) NH_3 flow rate

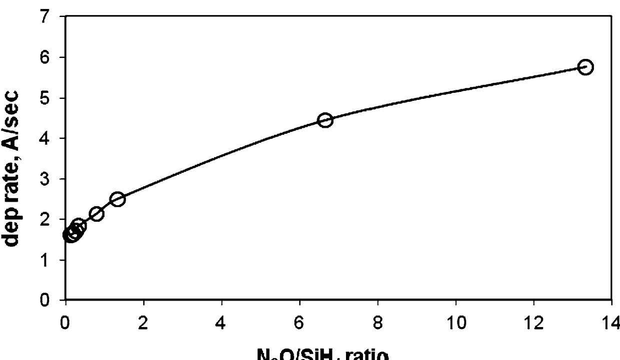


Fig. 54 PECVD SiO_xN_y deposition rate as a function of N_2O/SiH_4 ratio. (325 mTorr, 250 °C, 75 sccm SiH_4, 25 sccm NH_3, and varied N_2O flow)

Ion beam etching (IBE) and end-point

IBE is a physical sputtering process, which relies on the momentum transfer from the energetic ions (usually Ar) to the target material atoms. There exists a minimum ion energy threshold, above which the target material removal starts. Usually the energy used for IBE is a few tens electron volt to a few hundred electron volt. High beam energy results in a faster target material removal rate and more damage to the defined device [40].

During such material removal process, it is important to have a precise control on which layer to stop without impacting on its under layers (i.e., good selectivity), particularly for a multiple layer stack device. This requires sensitive end-point detection and accurate over-etch control (either by time or by selected signal amplitude). There are two general types of end-point detection approaches: (1) optical emission spectroscopy (OES). A specific element in a material stack with high optical emission intensity (such as Cu, Ni, Al, etc.) is usually chosen for this purpose (see Table 6). (2) Secondary ion mass spectroscopy (SIMS). This method is more versatile and has good detection capability for nearly all the elements above He, but it is more expensive than OES and requires a better vacuum than an OES system. Figure 56 shows Ta, Ru, and NiFe traces detected in a multilayer device stack. The top

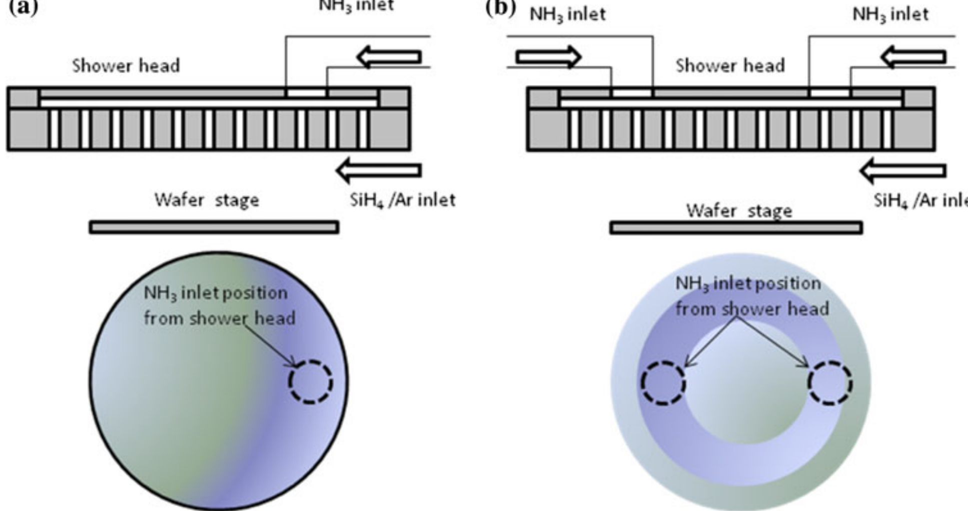


Fig. 55 Effect of shower head design on the SiN film thickness. (**a**) Single NH_3 inlet port; (**b**) double symmetrical NH_3 inlet port. RF power = 700 W, substrate temperature = 110 °C; SiH_4:Ar:NH_3 = 15:20:50 sccm, pressure = 120 mTorr

Table 6 Selected elements and their corresponding strongest emission lines which could be used for end-point detection during IBE

Elements	Wavelength (nm)
Al	396.1
Al	394.4
Cu	324.8
Cu	327.4
Mn	403.1
Mn	403.3
Ni	341.5
Ni	349.2
Ru	349.9
Ru	343.7

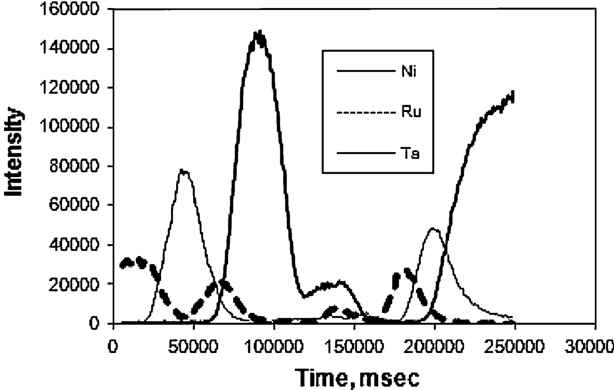


Fig. 56 SIMS end-point trace for a material stack containing Ru/Ta/Ru/NiFe…/Ru/Ta/NiFe multilayer structure. The IBE process was designed to stop after bottom Ta signal fall and start to flat or the bottom NiFe signal rising and start to flat

and bottom Ta is about 3 and 1.5 nm, respectively, and the SIMS has successfully detected the bottom Ta signal and triggered IBE to stop after the Ta intensity falls and stays flat. Certainly the signal intensity depends on the layer thickness and material removal rate, but high material removal rate will result in less control on over-etch amount for ultra thin film stacks.

Reactive ion etching (RIE)

Etching chemistry

Compared with the pure physical material removal in IBE, RIE utilizes both physical and chemical material removal mechanisms. With the correct selection of etching chemistry, hard mask, and process parameters (pressure, temperature, and bias), RIE provides more control in terms of the etching selectivity and final device profile.

Fluorine-based chemistry has been widely used for Si-based material (SiO_2, SiN, SiON, SiC, etc.) etching, while chlorine-based chemistry is more effective for etching aluminum, AlN, Al_2O_3, InP, GaN, InN, etc. [41]. Special handling is required for some etching gases whose boiling points are close to room temperature, thereby having a high risk of forming the liquid phase and clogging both gas delivery lines and mass flow controllers (MFCs) [42]. For example, BCl_3 has a boiling point of 12.5 °C. Typically, the gas line temperature should increase downstream from the cylinder to the processing chamber by at least 2 °C, i.e., to 23 °C in the fab, while keeping the cylinder at 21 °C by using an accurate temperature control jacket around the cylinder and gas line.

Another important aspect of BCl_3 chemistry is that it is very sensitive to oxygen and water moisture [43]. Oxygen/water will preferentially react with BCl_3 and forms boron oxide and this is the reason why the O (778 nm)/Ar (812 nm) OES peak ratio is constant below ~40 vol.% of O_2, while most of the BCl_3 is consumed and the O_2 content starts to increase above 40% of oxygen in the test shown in Fig. 57. Such an O_2-scavenging effect is obvious by comparing the oxygen content in the Cl_2–Ar–O_2 chemistry system for the same ICP plasma reactor under identical conditions in Fig. 58. It is very clear that the O (778 nm) OES intensity to Ar (812 nm) OES intensity ratio increases almost linearly with the oxygen content in the Cl_2–Ar–O_2 system. The O/Ar curve does not intercept at zero on the *Y*-axis in Figs. 57 and 58 when the oxygen flow was zero. This is due to the residual oxygen in the system.

End-point

As we discussed that the precise control of the etching stopping layer is critical for a nano-device definition with multilayer structure. An end-point can be defined by the falling signal from the layer component to be removed or by the rising signal of its under-layer material component.

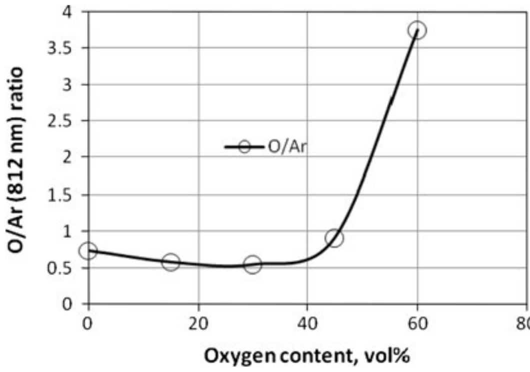


Fig. 57 O/Ar intensity ratio as a function of the oxygen volume percentage using (19-x)BCl_3-1Ar-$x$$O_2$ etching chemistry, 50 W bias power and 600 W source power on an Al_2O_3 substrate

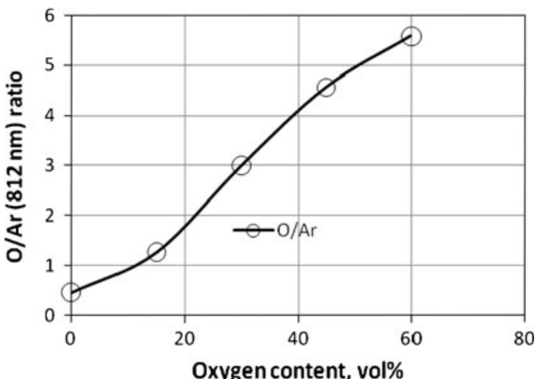


Fig. 58 O/Ar intensity ratio as a function of the oxygen volume percentage using (19-x)Cl_2-1Ar-$x$$O_2$ etching chemistry, 50 W bias power and 600 W source power on an Al_2O_3 substrate. O/Ar intensity ratio increases linearly with O_2, indicating non-O_2 scavenging effect of Cl_2

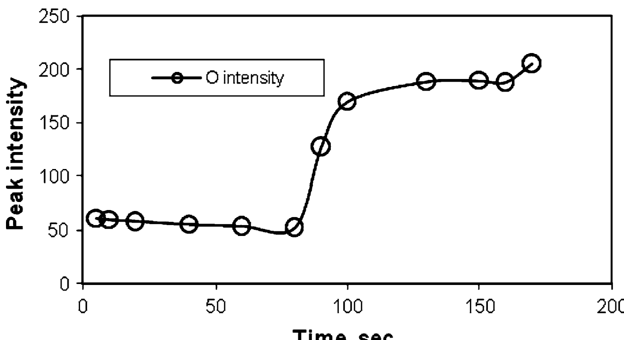


Fig. 59 End-point by O (778 nm) intensity rising for carbon etching at He–6O_2 gas combination (3 mTorr, source power = 600 W, bias power = 30 W)

Alternatively, the intensity of a reactant species or the etch byproducts can be used for end-point detection.

Figure 59 shows the oxygen OES peak at 778 nm as a function of etching time during the etching of amorphous carbon deposited on the CoFe film. SiO_xN_y is used as the hard mask here as it is not reactive towards the O_2–He chemistry. Since oxygen is largely consumed by reacting with carbon during the early stage of RIE, the O peak intensity is low and flat. Once the amorphous carbon layer is completely removed in the open area (not covered by the SiO_xN_y hard mask), the oxygen concentration from the gas phase will increase since no carbon will consume oxygen. Such a reactant component intensity increase can be a good end-pointing signal.

However, any plasma instability/arcing will cause OES or end-point signal fluctuation and may trigger an earlier end-point than designed. For example, in Fig. 60, the arcing in the IBE beam source triggered a Ni intensity drop at about 180 s. If Ni falling is used as an end-point, it could result in early detection of etching process completion and

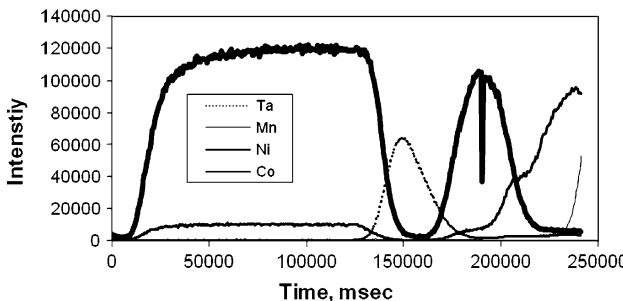


Fig. 60 Ion beam arcing caused Ni signal dipping at ~190 ms. (Beam conditions: 200 V/−2500 V grid 1/grid 2 voltage, 380 mA beam current, 7 sccm Ar)

lead to under-etched devices, i.e., the Ni layer is not fully removed at the time etching has been stopped. Therefore, it is critical to maintain a stable plasma source during both IBE and RIE.

Edge damage and geometry control

Physical versus chemical etching

In an RIE process, the reactive species react in both lateral (Eq. 19) and vertical (Eq. 20) directions.

$$R_{\Leftrightarrow} \propto J_{\Leftrightarrow} \times E_{\Leftrightarrow} \times e^{\frac{-E_a}{kT}} \tag{19}$$

$$R_{\Downarrow} \propto J_{\Downarrow} \times E_{\Downarrow} \times e^{\frac{-E_a}{kT}} \tag{20}$$

where R is the etch rate, J is the reactive species flux, E is the energy, and E_a is the reaction activation energy, T is the substrate temperature.

Figure 61 depicted how the above two component affects the profile of an etched device, depending on their relative magnitude. For most isolated feature etching, it is preferable to have a vertical post-etched profile, i.e., rate from Eq. 20 $\gg$ rate from Eq. 19. This can be achieved by (1) slowing down the thermal drift of the reactive etching species laterally, via sidewall passivation and lowered substrate temperature; (2) increasing the etch rate in the vertical direction, via increased ion bombardment, accelerated the removal of etching by-product at the bottom of device by raising substrate temperature, etc.

Bias effect

Figure 62 clearly demonstrated that increasing the bias power from 30 to 100 W changes the SiC profile towards more vertical. However, the hard masking corner rounding is a concern at higher bias voltage, this could result in faceting of the etched device if the mask is not thick enough and potentially causes other defects, such as "notching", which we will discuss in a later section.

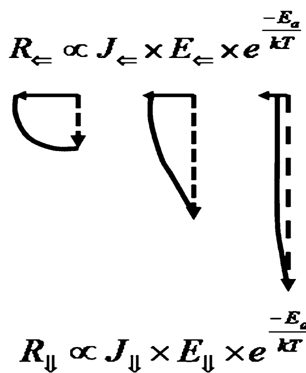


Fig. 61 Effect of vertical and lateral etching rate on the profile evolution

Increasing substrate biasing accelerates the removal of etching byproducts, similar to raising the temperature. For example, during Al_2O_3 etching, Cl is unlikely to react with Al_2O_3 and form $AlCl_3$ due to the very close bonding energy between Al–Cl and Al–O bonds. Therefore, BCl_3 needs to break the Al–O bond and form a pure Al layer (Eq. 21), which can be subsequently etched by Cl ions/radicals and form $AlCl_3$ [44].

$$BCl_3 + Al_2O_3 \Rightarrow B_2O_3(s) + B_3Cl_3O_3(g) + AlCl_3(s) + Al + Cl^+ \quad (21)$$

$$BCl_3 + B_2O_3(s) \Rightarrow B_3Cl_3O_3(g) \quad (22)$$

$$Al + Cl_2 \Rightarrow AlCl_3 \quad (23)$$

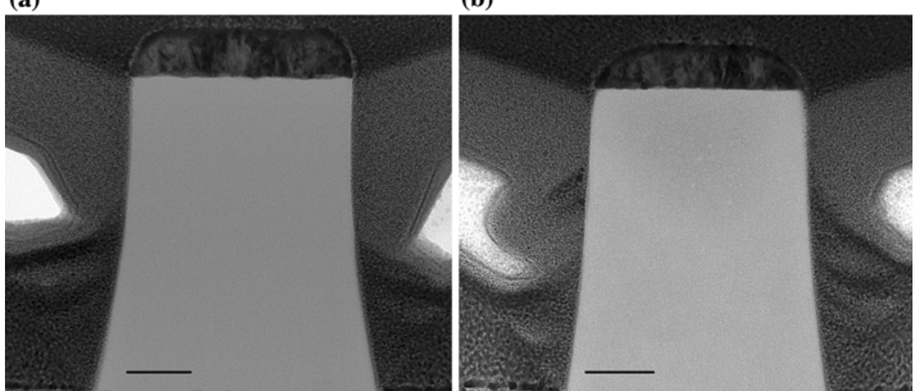
Similar oxide reduction initiation has been proposed for the etching of RuO_2 using BCl_3 chemistry by Kim et al. [45]. As B_2O_3 is thermodynamically stable and less volatile, compared with the etching byproducts for Si-based inorganic materials using F-based chemistry, ion bombardment is thus required to accelerate the removal of this B_2O_3 etch by-product and to enable the Al_2O_3 etching process to continue. From Eq. 22, the build-up of the B_2O_3 on the chamber wall could also consume BCl_3 content and reduce the Al_2O_3 etching rate. A wet chamber cleaning to remove the B_2O_3 build-up is necessary once the etching rate drops down to some threshold. While the removal of etch by-product can be accelerated by stronger ion bombardment, temperature is also very effect to boost the vapor pressure for $AlCl_3$ as discussed below.

Pressure and temperature effect

In addition to the bias voltage, pressure, and temperature are two other important parameters in controlling the etching rate and device profile. Referring to Eqs. 19 and 20, lowering the substrate temperature or pressure may be beneficial to avoid the isotropic etching if the reactive species have high thermal energy and/or easily react with the material on the sidewall; while if the etching process is limited by the surface reaction, increasing the temperature and/or the ion bombardment will certainly help to increase the etch directionality.

Higher pressure not only increases the ion scattering probability (and hence favors a sloped etched profile) when they travel across the sheath region, it also affects the etching rate. As both F-based and Cl-based gases have large electron affinity [46], significant amounts of electrons can be consumed via electron attachment to the neutral molecules and form negative ions. As a result, electron/plasma density in such chemistries (O_2, SF_6, Cl_2, etc.) drops with increasing process pressure [48, 49] and reduces the etching rate [50]. Figure 63 shows the normalized pressure and temperature effect on the wall angle of an isolated Al_2O_3 features etched using BCl_3 chemistry at 250 W bias power and 1750 W source power. Cr or NiCr has been used as the hard mask. Clearly, a process window exists for both temperature and pressure where a nearly vertical feature can be achieved. Generally, raising the substrate temperature does not only make the etch profile more vertical, but also improves the etching rate. Heiman et al. [51] found that at room temperature (300 K), the etch by-product ($AlCl_3$) has very low vapor pressure

Fig. 62 Source power = 600 W, pressure = 1 mTorr and etching gas = $15SF_6 + 15O_2$. 30 W bias power (**a**) vs. 100 W bias power (**b**) for SiC etching. Ni mask is used here. *Scale bar* = 100 nm



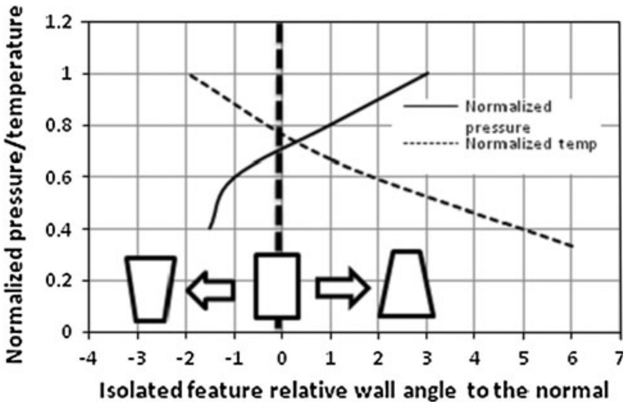


Fig. 63 Normalized substrate temperature and chamber pressure effect on the profile of etched Al_2O_3 features

($\sim 10^{-4}$ Torr); while at 150 °C (423 K), the vapor pressure increases to $\sim$85 Torr (Eq. 24) and the etch by-product is sufficiently volatile. Tokunaga and Hess [52] also found that the etch rate markedly increased at elevated substrate temperature. Interestingly, increasing the bias voltage from −500 to −750 V did not significantly raise the etch rate of Al_2O_3, indicating that the etching is largely chemically induced.

$$P_{AlCl_3} = \exp\left(37.2 - \frac{13860}{T}\right) \quad (24)$$

Therefore, it is important to keep the wafer stage at the desired temperature with minimum variation. This can be achieved by electro-static chucking (ESC) or by mechanically clamping the wafers onto a stage, whose temperature is controlled by a chiller/heater. Some caution must be exercised, however, when dealing with the wafer clamping, particularly when ESC is used. Particles on the ESC chuck or on the back or edge of a wafer result in poor wafer chucking and uneven backside heating/cooling and high He leaking.

For a unipolar ESC system, after the plasma is off, the wafer stage is lowered down and if the ESC chuck is not fully discharged, cracking of wafers could result (see Fig. 64). This can been resolved by slowing down the initial stage downwards-moving speed (or unloading pin upwards moving speed) and thus provides long enough time for the ESC to discharge as shown on right hand side of Fig. 64.

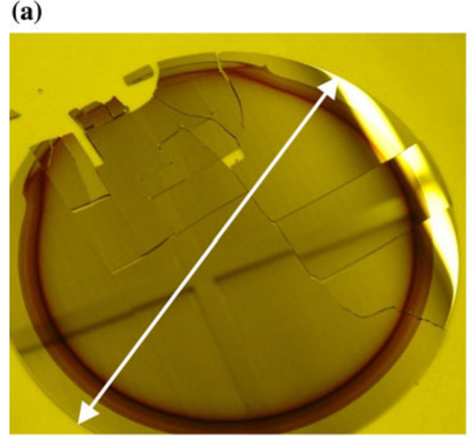
Notching due to ion deflection

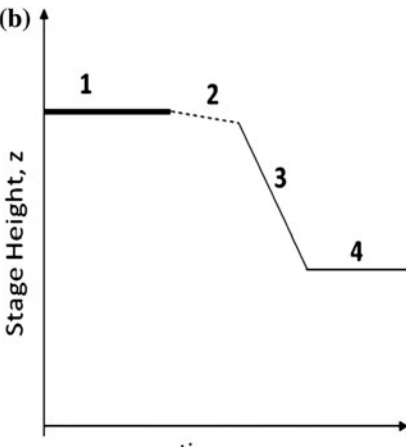
Notching is a common defective profile for IBE/RIE defined features. Ion scattering within the sheath due to higher pressure will change the ion trajectory and leads the ions to bombard the surface with angled incidence. Such shallow-angled incident ions are then deflected from the side wall surface and hit the bottom of the etched features. Consequently, a notch is formed (see Fig. 65a). The notching effect in RIE caused by ion deflection is enhanced at higher pressure and larger substrate biasing. Mask faceting and a sloped device feature profile can further accelerate such notching due to the deflection of incoming ions after impinging onto the sloped surface for both IBE and RIE processes.

Such notching is detrimental as it punches through the under layers locally and needs to be avoided. The ion defection can be minimized by reducing the ion scattering across the sheath region for RIE. Reducing the bias voltage prior to the etching end-point helps to minimize the notching. With process optimization, an ideal profile with a straight wall angle as shown in Fig. 65b can be achieved.

Since such notching defects have been observed not only for insulating material etching (such as the amorphous carbon in Fig. 65a) but also for metallic materials stack etching as shown in Fig. 66, it is therefore unlikely that the notching in Fig. 65 is “solely” caused by the charging-related ion trajectory change as we will discuss later. For a magnetic tunneling junction in particular, minimizing such

Fig. 64 (**a**) Wafer cracking due to inappropriate ESC de-chucking operation and (**b**) the corrected de-chucking procedures to avoid this. *1* Process position, *2*: initial stage downwards (slow motion), *3* fast stage moving towards final position, *4* final stage position. *Arrow* = 150 mm





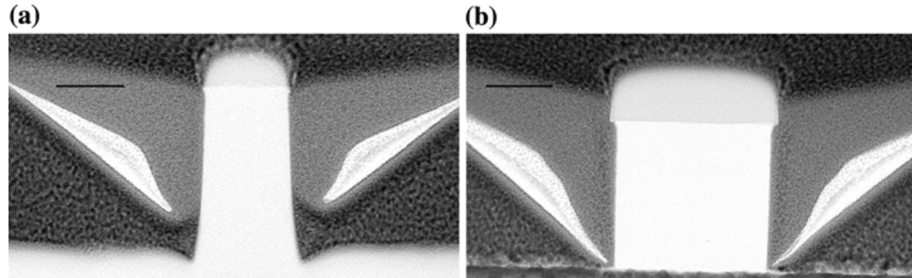


Fig. 65 TEM images of partially etched carbon profile with notching (**a**) and a fully etched carbon layers with straight wall (**b**) (reproduced from [29]). *Scale bar* = 100 nm

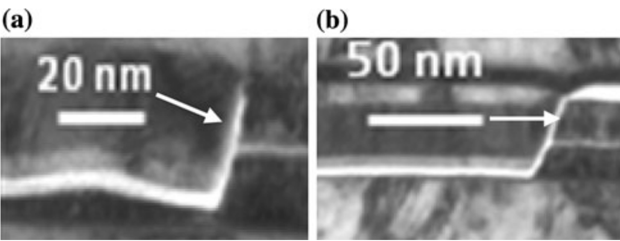


Fig. 66 (**a**) "Notching" formed at the bottom of a TMR device. (**b**) A perfect flat top and bottom device (the mask is intentionally left here to increase the imaging contrast on top of the device here). The *arrows* in the images indicate the hard bias magnetic field direction in the corresponding devices due to the junction profile changes

notching is critical, since a "notched" junction causes the hard biasing field to tilt towards the bottom. This results in an undesired weakly and/or asymmetrically biased magnetic free layer, compared with a normally biased free layer for devices without notching defects as shown in Fig. 66b. Ideally, we prefer to have the hard biasing field parallel to the free layer (the layer above the white line in the graph).

Similar to ion deflection, electron shadowing may also result in "notching", but mostly for insulator film stack etching. The electron flux is more or less isotropic due to its low energy and directionality, compared with the ion flux (which impinges perpendicular to the substrate surface). For a high aspect ratio trench or via, the electrons therefore tend to accumulate on the top portion of insulator features, while positive charges due to ion bombardment will build-up at the bottom of such features [53–56]. This creates a local electric field pointing from the bottom to the side wall of the trench/via and deflects the incoming ion trajectory towards the corner of a trench/via (see Fig. 67) [57]. Okamoto [53, 54] studied etched SiC profiles due to ion defection and electron shadowing for n-type SiC and semiconducting type SiC in $SF_6 + O_2$ chemistry, as deep as 10 µm trenching has been observed due to such electron shadowing.

Symmetrical profile control

For small dimension device patterning, the photo-resist (PR) mechanical stability deteriorates as its aspect ratio

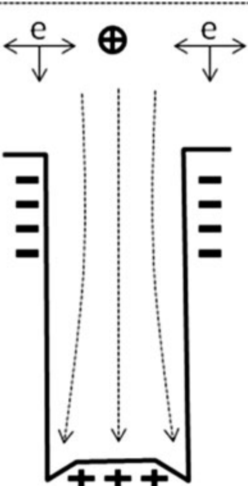


Fig. 67 Sketch showing the electron shadowing impact on the incoming ion trajectory and the resulted etching profile changes when etch insulator layers. The charge building up causes the scattering of the ions and the resulted undercut at the corner (reproduced from [57], with permission)

increases [58]. Consequently, a tilted device profile as shown in Fig. 68b could result. One of the approaches to solve this problem is using inorganic hard masks (such as metal, oxide, etc.) with high selectivity and thus short mask height. In methanol (CH_3OH) etching chemistry, a Ta hard mask can provide selectively from 5–10 relative to magnetic materials [40]. As a result, much shorter mask height is required and this gives a more symmetrical junction profile shown on Fig. 68a.

Edge damage control

The edge effect becomes more significant as the device becomes smaller. For example the magnetic reader sensor width is approaching ~15 nm (see Fig. 69a) for 1 Tb/in^2 storage capacity, a damaged layer as thick as a few nanometers has been observed on each side of a sensor (see Fig. 69b), which could account for up to ~20% of device width. Minimizing and controlling such edge damage are crucial for a nano-scale device fabrication. Device patterning using low beam energy IBE and less aggressive chemistry in RIE (such as CH_3OH compared with Cl-based

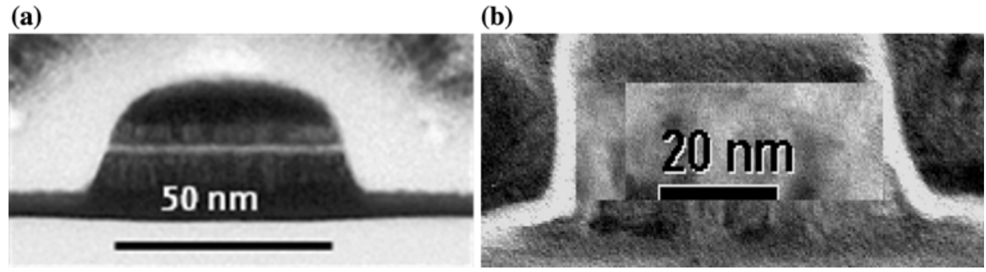


Fig. 68 TEM image of a RIE defined (using CH_3OH chemistry) TMR sensor cross-section showing symmetrical profile (**a**) (reproduced from [40] with permission); TEM image of an IBE defined device junction with asymmetrical profile (**b**) (reproduced from [58], with permission)

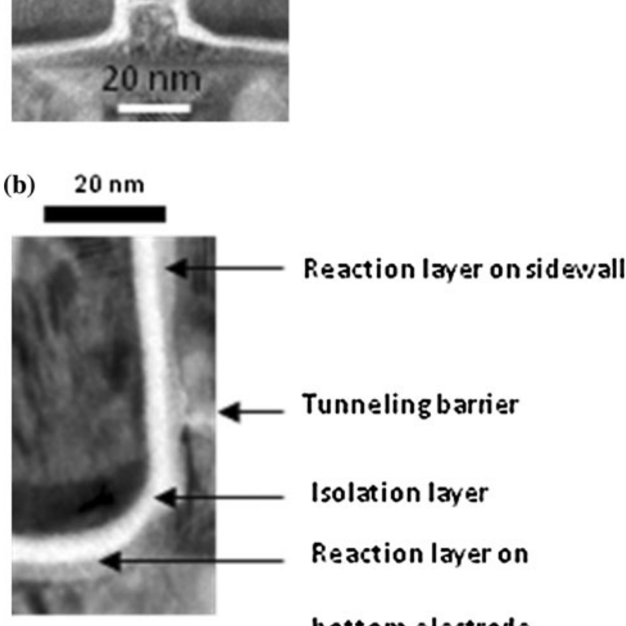


Fig. 69 (**a**) A 15 nm device cross-section TEM image; (**b**) a portion of the device showing the edge reaction layer (reproduced from [40] with permission)

chemistry, etc.) can be beneficial. Non-oxide based isolation layer (SiN) encapsulation immediately following the junction formation can further minimize oxygen attack and corrosion in ambient of such a newly-formed surface and thus minimize the un-wanted edge damage and undesired oxide layer formation.

Corrosion issue of etched devices

When F-based and Cl-based chemistries are used in a conventional RIE process, the potential corrosion risk due to the possible entrapment of etching byproducts or etching agents needs to be carefully reviewed. Figure 70 shows the top down SEM images post-etching for various stacks, such as SiC/Ni/Ta, SiC/Cr, and CoFe/SiC/Ni (from bottom to top. Ta, Cr, Ni are used as hard mask here). Etching residuals and/or corrosion spots are clearly visible in Fig. 70a due to the low boiling point of TaF_5 (229 °C) formed from the reaction of Ta hard mask with F-based chemistry. As the wafer stage temp is set at ~80 °C, it is difficult to completely vaporize the TaF_5 during the etching of the SiC/Ni/Ta stack. As a result, TaF_5 re-deposits onto adjacent open areas. Figure 70b indicates that Cr is also susceptible to attack by F-chemistry and forms CrF_x, therefore, it is not a good mask material in F-chemistry (Ni is better). CoFe is even more susceptible to the corrosion caused by the F-residual after exposed to air, as this residual reacts with moisture and forms more corrosive HF (see Fig. 70c).

Similar precautions need to be exercised for Cl-based etching chemistry, since a Cl-residual on a wafer tends to react with moisture and forms corrosive HCl byproduct and attacks the surrounding materials. It is evident from Fig. 71a–c that a ~50 nm thick Cl-containing residual material was formed on an Al_2O_3 feature etched using BCl_3 chemistry after it is exposed to atmosphere without any post-etching treatment. By using O_2, H_2, water plasma treatment or water rinsing [59], or methanol plasma treatment [60], such a residual can be readily removed and thus the corrosion risk can be minimized.

Conclusions

In this review paper, the authors have elucidated some key features of plasmas used in the manufacture of devices. We have tried to illustrate the effectiveness of plasma-based process in device manufacture, and the means by which those processes can be optimized. In particular we would like to highlight the following conclusions:

Plasma sources

To balance the plasma density and uniformity requirements, operation flexibility and system cost, proper selection of a plasma source to suit a particular application is critical. ICP and CCP (13.56 MHz vs. >30 MHz UHF) are

Fig. 70 (**a**) Re-deposited TaF_5 by-product post-etching of SiC/Ni/Ta stack; (**b**) Cr mask attacked by F-chemistry in SiC/Cr stack; and (**c**) CoFe layer corrosion spots in a CoFe/SiC/Ni stack post-etching. Etch gas = SF_6. *Scale bar* = 1 μm for (**a**)–(**b**) and 100 μm for (**c**)

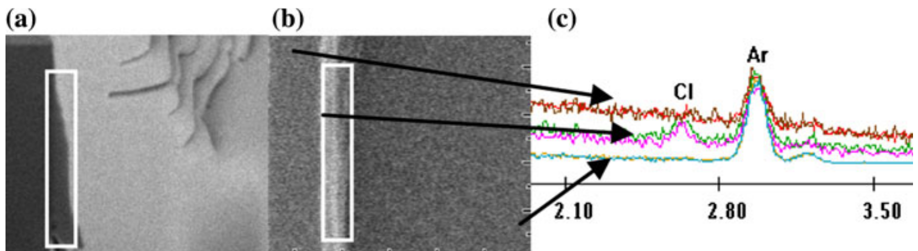


Fig. 71 Cross-section (**a**), top down view (**b**), and the corresponding energy dispersion spectra (**c**) of the selected areas from top down image for an Al_2O_3 feature etched in BCl_3 chemistry. The width of the white box = 50 nm for left and middle images; the *X*-axis is the energy in keV for EDS spectra graph in (**c**). Ar peak is due to the entrapped gas from sputtered Al_2O_3 layer (using Ar as the working gas)

still the two major commercial plasma sources. Due to different plasma sustaining mechanisms, both ICP and UHF CCP offer higher plasma density, lower plasma potential, and electron energy at the same external input power levels, compared with a 13.56 MHz CCP source. This is important for some applications requiring lower plasma induced damage and contamination due to the ion bombardment of the plasma surroundings.

Thin film deposition

Thin film deposition can be achieved via a variety of plasma-based process, such as magnetron sputtering, IBD, and PECVD.

Magnetron sputtering is one of the most commonly employed commercial thin film deposition process. Designs incorporating a tilted target (relative to the substrate normal) offer significant advantages to the achievement of uniform film deposition on large substrate surfaces with a relatively small target size and reasonable target–substrate separation. They can be used to create a film thickness "wedge" for fast evaluation of the impact of thickness on critical stack layers. To be effective in trapping electrons, the fringe magnetic field on top of the target surface should be more than 300 G. Therefore, properly matching target thickness and magnetron strength is important to ensure the effectiveness of a magnetron. Magnetron development is vital to maintain uniform target erosion and higher target utilization without compromising the film uniformity at the end of target life. Ideally, a well-designed magnetron enables magnetron position adjustment to enable a stable target surface fringe field as the target erodes. Minimizing the fringing field from the magnetron going through the substrate surface perpendicularly (electrons follow the magnetic field lines and thus the ionization) is vital to avoid excessive ion bombardment and helps to prevent the ion-induced damage of the growing films. This can be achieved either by magnetron design itself, by proper arrangement of the adjacent magnetron, or by using magnetic field shielding around the substrate stage.

For sputter deposition of dielectric films, maintaining a constant substrate/cathode surface area will minimize the deposition rate drift due to conducting area change for chamber wall, wafer stage, and shielding. "Flashing" with a metal layer at some pre-defined frequency can help to maintain good wafer to wafer deposition rate.

For IBD deposition, the plasma is usually generated with an ICP source with Ar as the inert working gas and the ions are then extracted from the grid sets to achieve the desired beam energy, current, and divergence angles. The deposited film uniformity largely depends on the ejected atom flux angle relative to the substrate normal, which in turn also depends on the beam angle and beam voltage. Understanding the angular distribution profile (cosine, over cosine, or under cosine, etc.) of the ejected atom flux from a target surface is critical for film uniformity and composition control. Generally, keeping the incident atom flux at an angle relative to the substrate normal helps to improve the film uniformity (just like the tilted target design in

magnetron sputtering). However, this can lower the deposition rate a little.

In PECVD film deposition processes, both mass transportation and surface diffusion/reaction are critical to control the film growth rate and uniformity. Maintaining a uniform gas flow (via a suitable shower head design and associated pumping) is important for film uniformity control; while the substrate stage temperature has a strong impact on film microstructure and uniformity.

Thin film etching

The ultimate goal of thin film etching is to achieve a controllable device profile with minimal damage to the film.

For an IBE defined device, its profile will largely depend on the mask height, material selection, and beam angle relative to the substrate normal. All these parameters determine the shadowing effect and re-deposition amount. Generally, a shorter mask enables less shadowing effect at a fixed beam angle; while a vertical incident beam gives a straighter device profile, but has more re-deposition around the mask.

Although IBE is versatile in this aspect due to the fact that it removes the material via physical sputtering, it usually does not provide good selectivity. Furthermore, intermixing and device edge damage are not easy to control, particularly at high etching rates (higher beam energy and current).

The device profile dependence on process parameters in RIE is more complex due to the existence of both chemical and physical components in the etching process. However, RIE can provide better selectivity, compared with the IBE.

Minimizing the lateral etching rate and increasing the vertical one generates a more uniform vertical profile. Temperature, pressure, bias voltage, and mask erosion all affect the patterned device profile development. Temperature could be favorable or unfavorable to the desired vertical profile, depending on whether it preferentially increases the vertical etching component or the lateral etching component; while lower pressure usually favors a more vertical profile due to the reduced ion scattering across the ion sheath region. Both ion deflection from the side wall of etched features and the charge-induced electric field bending could cause notching defects. However, careful post-etching treatments (by O, H, R-OH plasmas or deionized water-DI rinse) are usually required to remove any potential etching byproducts/residuals (such as F, Cl, S-containing species) and to avoid the corrosion of the finished devices.

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